GM82C803C

2.88 MB FDC/ Dual UARTs with FIFO/
PIO(EPP/ ECP)/ IDE Interface/ S-IR/ PnP

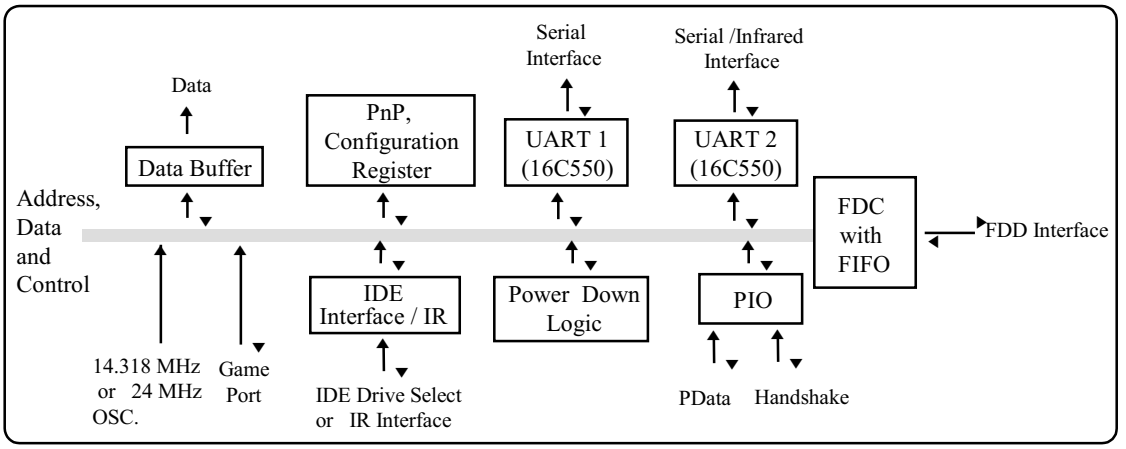
General Description

The GM82C803C is a single 100-pin PC95 compatible Super I/O chip with a Floppy Disk Controller with data separator, two UARTs (GM16C550) and an infrared interface, one Parallel port (IEEE 1284 Compliant). The GM82C803C is optimized for motherboard applications. The GM82C803C also includes one game port selection, IDE interface and an address decoder for on-chip function. The Floppy Disk Control part provides all the needed functionality between the host processor peripheral bus and the cable connector to the Floppy Disk Driver. It integrates the selection, clock generation and high current drivers and supports the 4 MB drive as well as the other standard drives. The UARTs on GM82C803C are compatible with the 16C550. One UART (COM2) includes Serial Infrared Interface, complying with IrDA, HPSIR, and ASKIR streams. The Configuration register is used to allocate the I/O Base Address IRQ or DMA for each corresponding function.

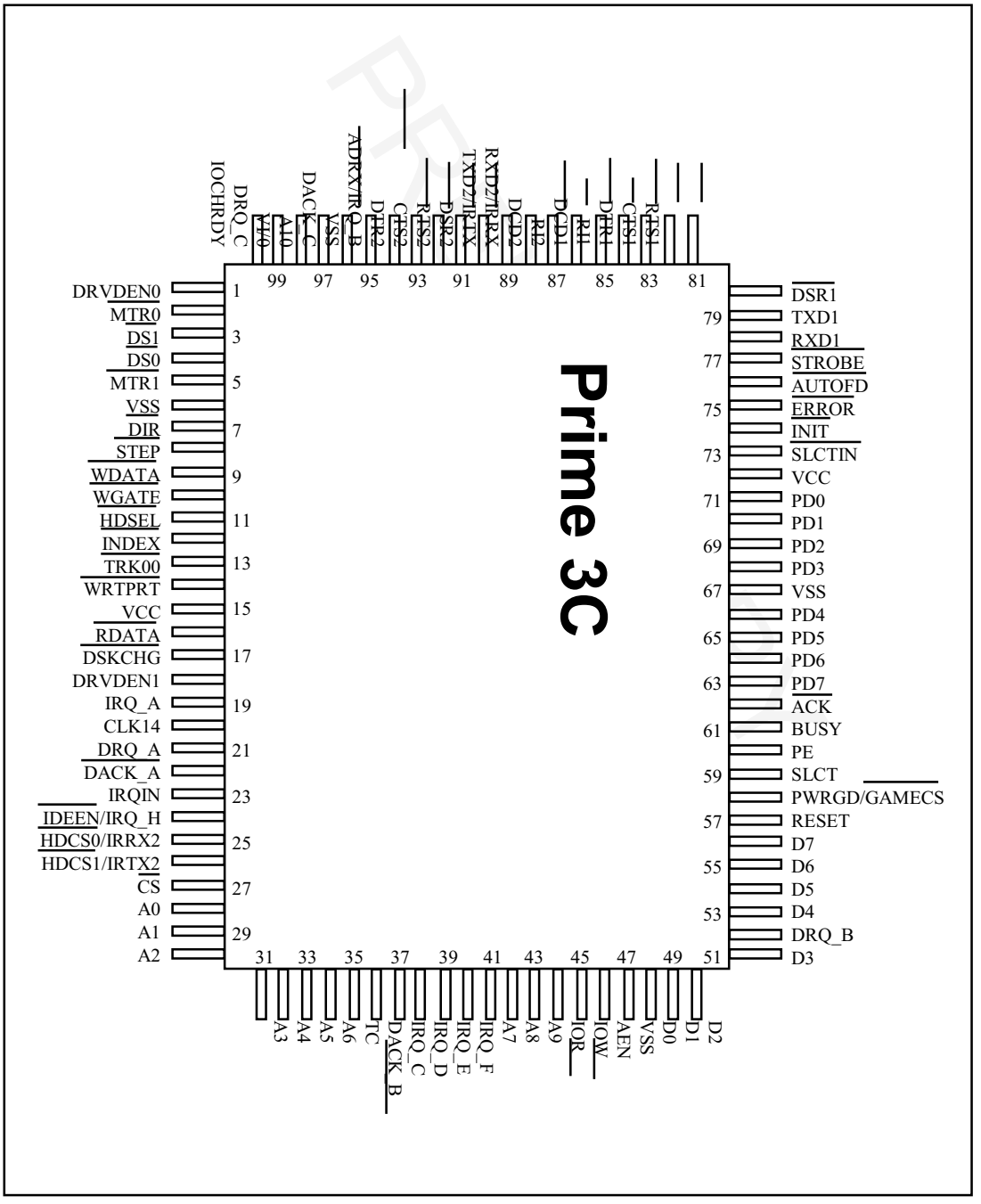
Features

- 100% Hardware compatible to the IBM PC/AT
- Floppy Disk Controller with 16 bytes FIFO (default disable)
  - Data rates up to 1Mbps
  - Perpendicular recording drive support
  - Drives up to two FDDs
  - 40 mA floppy disk drive interface
  - FDD swap
  - 48 Base I/O addresses, 7 IRQ and 3 DMA options
- Dual UARTs compatible to the GM16C550
  - Programmable character lengths (5, 6, 7, 8)
  - Even, odd, stick or no parity bit generation and detection
  - Programmable baud rate generator
  - High speed baud rate (230 Kbps, 460 Kbps) support
  - Independent transmit/ receiver FIFOs
  - MIDI interface
  - Modem control
  - Infrared -IrDA(HPSIR) and ASK(Amplitude Shift Keyed)IR
  - Optional alternate IR pins
  - 96 Base I/O addresses and 7 IRQ options
- Multi-mode parallel port
  - Standard mode
  - ECP (IEEE 1284)
  - EPP (Version 1.9 : default, Version 1.7)
  - 192 Base I/O addresses, 7 IRQ and 3 DMA options
- IDE interface (optional)
  - 48 Base I/O addresses and 7 IRQ options
- Game chip selection logic
  - 48 Base I/O addresses
- General Purpose Address Decoder
  - 48 Base I/O addresses
- Power Down support
- 5 Volt operation
- 14.318 MHz or 24 MHz clock
- 100 pin QFP

Internal Block Diagram



1. Pin Configuration



2. Pin Description

PIN NO.	PIN NAME	BUFFER TYPE	DESCRIPTION
			1) HOST INTERFACE
19, 37-40	IRQ_A IRQ_C IRQ_D IRQ_E IRQ_F	Out	Interrupt Request pin. The interrupt request from the logical device or IRQIN is output on one of the IRQA-G signals. Refer to the configuration registers for more information. If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.
21,52, 99	DRQ_A DRQ_B DRQ_C	Out	DMA Request pin. This active high output is the DMA request for byte transfers of data between the host and the chip. This signal is cleared on the last byte of the data transfer by the $\overline{\text{DACK}}$ signal going low (or by $\overline{\text{IOR}}$ going low if $\overline{\text{DACK}}$ was already low as in demand mode).
22,36, 96	$\overline{\text{DACK}}$_A $\overline{\text{DACK}}$_B DACK_C	In	DMA Acknowledge pin. This active low input acknowledging the request for a DMA transfer of data between the host and the chip. This input enables the DMA read or write internally.
27	$\overline{\text{CS}}$	In	Chip Select pin. When enabled, this active low pin serves as an input for an external decoder circuit which is used to qualify address lines above A10.
28-34 41-43, 97	A0-A10	In	I/O Address pin. These host address bits determine the I/O address to be accessed during $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$ cycles. These bits are latched internally by the leading edge of $\overline{\text{IOR}}$ and $\overline{\text{IOW}}$. All internal address decodes use the full A0 to A10 address bits.
35	TC	In	Terminal Count pin. This signal indicates to the chip that DMA data transfer is complete. TC is only accepted when $\overline{\text{DACK}}$_x is low. TC is active high.
44	$\overline{\text{IOR}}$	In	I/O Read pin. This active low signal is issued by the host microprocessor to indicate a read operation.
45	$\overline{\text{IOW}}$	In	I/O Write pin. This active low signal is issued by the host microprocessor to indicate a write operation.
46	AEN	In	Address Enable pin. Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
48-51 53-56	D0-D7	In/Out	Data Bus 0-7. This data bus used by the host microprocessor to transmit data to and to receive from the chip. These pins are in a high- impedance state when not in the output mode.
57	RESET	In	This active high signal resets the chip and must be valid for 500ns minimum. The affect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.

(Continued)

PIN NO.	PIN NAME	BUFFER TYPE	DESCRIPTION
2) FLOPPY DISK INTERFACE			
1	DRVD-EN0	Out	Indicates the drive and media selected.
2, 5	$\overline{\text{MTR0}}$, MTR1	Out	Motor On 0,1 pins. These active low open drain outputs select motor drives 0-1.
3, 4	$\overline{\text{DS1}}$, DS0	Out	Drive Select pin. Active low open drain outputs select drives 0-1.
7	$\overline{\text{DIR}}$	Out	Direction Control pin. This high current low active output determines the direction of the head movement. A logic 1 on this pin means outward motion, while a logic 0 means inward motion.
8	$\overline{\text{STEP}}$	Out	Step Pulse pin. This active low high current driver issues a low pulse for each track-to-track movement of the head
9	$\overline{\text{WDATA}}$	Out	Write Data pin. This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
10	$\overline{\text{WGATE}}$	Out	Write Gate pin. This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
11	$\overline{\text{HDSEL}}$	Out	Head Select pin. This high current output selects the floppy disk side for reading or writing. A logic 1 on this pin means side 0 will be accessed, while a logic 0 means side 1 will be accessed.
12	$\overline{\text{INDEX}}$	In	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
13	$\overline{\text{TRK00}}$	In	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
14	$\overline{\text{WRTPRT}}$	In	Write Protected pin. This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
16	$\overline{\text{RDATA}}$	In	Read Disk Data pin. Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
17	$\overline{\text{DSKCHG}}$	In	Disk Change pin. This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
18	DRVDEN1	Out	Indicates the drive and media selected.

(Continued)

PIN NO.	PIN NAME	BUFFER TYPE	DESCRIPTION
		3) SERIAL PORT INTERFACE	
88	RXD2/ IRRX	In	Receive Data pin. Receiver serial data input for port 2. IR Receive Data.
89	TXD2/ IRTX	Out	Transmit Data pin. Receiver serial data output for port 2. IR Transmit Data.
78	RXD1	In	Receive Data pin. Receiver serial data input for port 1.
79	TXD1	Out	Transmit Data pin. Transmit serial data output for port 1.
81, 91	$\overline{\text{RTS1}}$, $\overline{\text{RTS2}}$	Out	Active low Request To Send outputs for the serial port. Handshake out put signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the RTS signal to inactive mode (high). Forced inactive during loop mode operation.
83, 93	$\overline{\text{DTR1}}$, $\overline{\text{DTR2}}$	Out	Active low Data Terminal Ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the $\overline{\text{DTR}}$ signal to inactive mode (high). Forced inactive during loop mode operation.
82, 92	$\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$	In	Active low Clear to Send inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTS signal by reading bit 4 of Modem Status Register (MSR). A CTS signal state change from low to high after the last MSR read will set MSR bit 0 to a logic 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTS changes state. The CTS signal has no effect on the transmitter. * Note : Bit 4 of MSR is the complement of CTS.
80, 90	$\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$	In	Active low Data Set Ready inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of $\overline{\text{DSR}}$ signal by reading bit 5 of Modem Status Register (MSR). A $\overline{\text{DSR}}$ signal state change from low to high after the last MSR read will set MSR bit 1 to a logic 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DSR}}$ changes state. * Note : Bit 7 of MSR is the complement of $\overline{\text{DSR}}$.
85, 87	$\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$	In	Active low Data Carrier Detect inputs for the serial port. Handshake signal which notifies the UART that the carrier signal detected by the modem. The CPU can monitor the status of $\overline{\text{DCD}}$ signal by reading bit 7 of Modem Status Register (MSR). A DCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DCD}}$ changes state. * Note : Bit 7 of MSR is the complement of $\overline{\text{DCD}}$.

(Continued)

PIN NO.	PIN NAME	BUFFER TYPE	DESCRIPTION
84, 86	$\overline{RI1}$, $\overline{RI2}$	In	Active low Ring Indicator inputs for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of $\overline{RI}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{RI}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a logic ?? If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{RI}$ changes state. * Note : Bit 6 of MSR is the complement of RI.
			4) PARALLEL PORT INTERFACE
73	$\overline{SLCTIN}$	In/Out	Printer Select Input pin. The active low output selects the printer. This is the complement of bit 3 of the Parallel Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
74	$\overline{INIT}$	In/Out	Initiate pin. This output is bit 2 of the Parallel Control Register. This is used to initiate the printer when low. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
76	$\overline{AUTOFD}$	In/Out	Autofeed pin. This output goes low to cause the printer to automatically feed one line after each line is printed. The $\overline{AUTOFD}$ output is the complement of bit 1 of the Parallel Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
77	$\overline{STROBE}$	In/Out	An active low pulse on this output is used to strobe the printer data into the printer. The $\overline{STROBE}$ output is the complement of bit 0 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
61	BUSY	In	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
62	$\overline{ACK}$	In	Acknowledge pin. A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
60	PE	In	Paper End. Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.

(Continued)

PIN NO.	PIN NAME	BUFFER TYPE	DESCRIPTION
59	SLCT	In	Printer Selected Status pin. This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
75	$\overline{\text{ERROR}}$	In	A low on this input from the printer indicates that there is an error condition at the printer. Bit 3 of the Printer Status register reads the $\overline{\text{ERR}}$ input . Refer to Parallel Port description for use of this pin in ECP and EPP mode.
63-66 68-71	PD7-PD0	In/Out	Port Data pin. The bi-directional parallel data bus is used to transfer information between the chip and peripherals.
100	IOCH-RDY	Out	In EPP mode, this pin is pulled low to extend the read/write command. This pin has an internal pull-up.
5) IDE/16 BIT ADDRESS QUALIFICATION/ ALT IR PINS			
24	$\overline{\text{IDEEN}}$ IRQ_H	In (Note) Out	IDE Enable pin. This active low signal is active when the IDE is enabled and the I/O address is accessing an IDE register. The interrupt request from a logical device or IRQIN may be output on the IRQ_H signal. Refer to the configuration registers for more information. If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.
25	$\overline{\text{HDCS0}}$ IRRX2	Out (Note) In	IDE Chip Select pin. This is the Hard Disk Chip select corresponding to the eight control block addresses. IR Receive pin. Alternate IR Receive input.
26	$\overline{\text{HDCS1}}$ IRTX2	Out (Note)	IDE Chip Select pin. This is the Hard Disk Chip select corresponding to the alternate status register. IR Transmit pin. Alternate IR Transmit output.
6) MISCELLANEOUS			
20	CLK14	ICLK	Clock pin. The external connection to a single source 14.318 MHz clock.
23	IRQIN	In	This pin is used to steer an interrupt signal from an external device onto one of eight IRQ outputs, IRQA-H.
58	PWRGD $\overline{\text{GAMECS}}$	In Out	This active high input indicates that the power (Vcc) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all outputs are put into high impedance. The contents of all registers are preserved as long as Vcc has a valid value. The driver current drain in this mode drops to ISTBY (standby current). This input has an internal pull-up. This is the Game Port Chip Select output active low. It will go active when the I/O address, qualified by AEN, matches that selected in Configuration Register GDR.

(Continued)

PIN NO.	PIN NAME	BUFFER TYPE	DESCRIPTION
94	$\overline{\text{ADRX}}$	Out	Address x pin. Active low address decode out; used to decode a 1, 8, or 16 byte address block. (An external pull-up is required). Refer to Configuration Registers (index=D6,D7) for more information. This pin has a 30 uA internal pull-up.
	IRQ_B	Out	The interrupt request from a logical device or IRQIN may be output on IRQ_B. Refer to the configuration registers for more information. (If EPP or ECP Mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.)
98	$V_{I/O}$		I/O Power pin. I/O Interface Supply Pin (5V).
15,72	Vcc		Positive Supply Voltage.
6,47, 67,95	GND		Ground Supply.

Note : When IDE and IRQ_H, IRRX2, IRTX2 are not selected, 3 μA pull-ups are active on the Pin 24, Pin 25, and Pin 26

Note : IDE does not decode for 377, 3F7

Note : RI and the Serial interrupt is always active if system power is applied to the chip.

3. CONFIGURATION

3.1 Configuration Register

The GM82C803C has configuration registers. The configuration registers can be set by software. Each configuration register is pointed by the value of the index register, and the contents of the configuration register is changed by writing data to the port 399H.

3.1.1 Device Identification Register (IDR : read only)

Index = C0

The contents of this is 3C for GM82C803C.

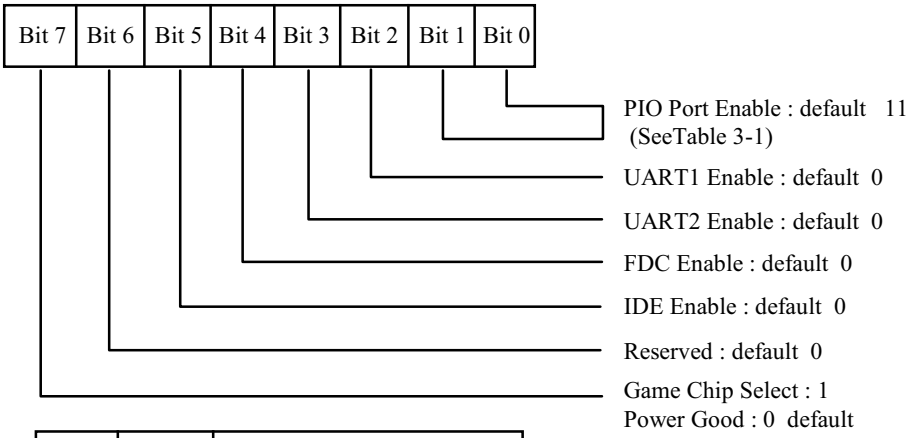
3.1.2 Device Revision Register (RVR : read only)

Index = C1

This indicates revision number, the default is 00

3.1.3 Function Selection Register (FSR)

Index = C2

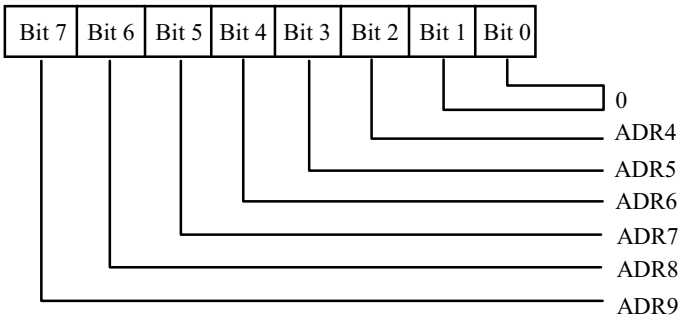


Bit 1	Bit 0	PIO Mode
0	0	Uni-directional Mode
0	1	ECP
1	0	EPP
1	1	PIO Disable

(Table 3-1 PIO Port Mode Selection)

3.1.4 FDC Address Register (FAR)

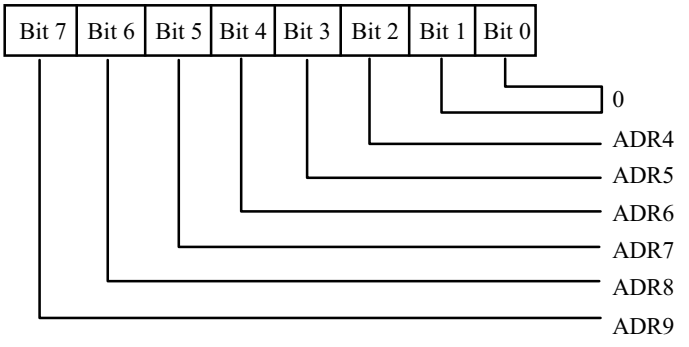
Index = C3



This register is used to select the base address of the Floppy Disk Controller.
The FDC can be set to 48 locations on 16 byte boundaries from 100H-3F0H.
Upper address decode requirements: CS = ??and A10 = ??are required to access the FDC registers.
A[3:0] are decoded as 0xxxb

3.1.5 IDE Base address Register (IBR)

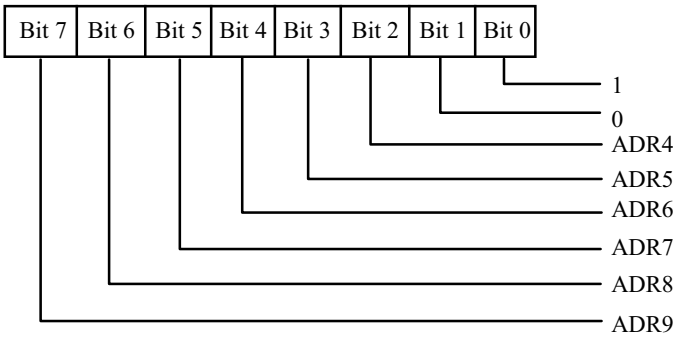
Index = C4



This register is used to select the base address of the IDE Interface Control Registers (0-7).
This can be set to 48 locations on 16byte boundaries from 100H-3F0H.
Upper address decode requirements: CS = ??and A10 = ??are required to access the IDE registers.
A[3:0] are decoded as 0xxxb

3.1.6 IDE Status address Register (ISR)

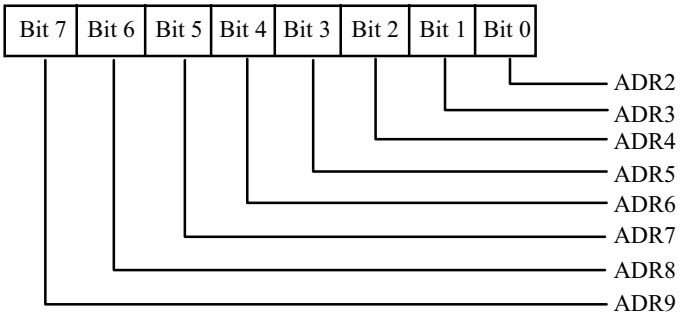
Index = C5



This register is used to select the base address of the IDE Interface Alternate Status Registers.
This can be set to 48 locations from 106H-3F6H.
Upper address decode requirements: CS = ??and A10 = ??are required to access the IDE registers.
A[3:0] must be 0110b

3.1.7 Parallel Port base Address Register (PAR)

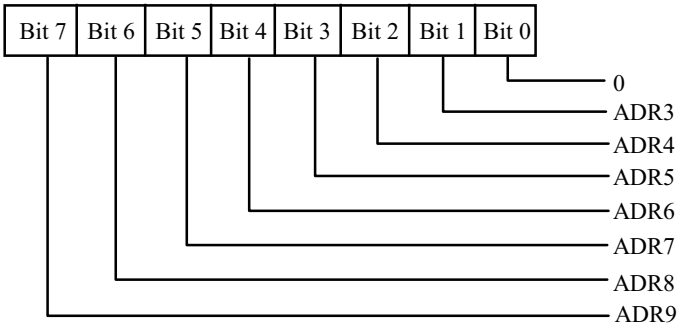
Index = C6



This register is used to select the base address of the parallel port.
If EPP is not enabled, the parallel port can be set to 192 locations, on 4 byte boundaries form 100h-3FCh.
If EPP is enabled, the parallel port can be set to 96 locations, on 8 byte boundaries from 100h-3F8h.
Upper address decode requirements : CS = ??and A10 =??are required to access the parallel port when not ECP mode. (A10 active : when in ECP mode)

3.1.8 First Serial port base address Register (FSR)

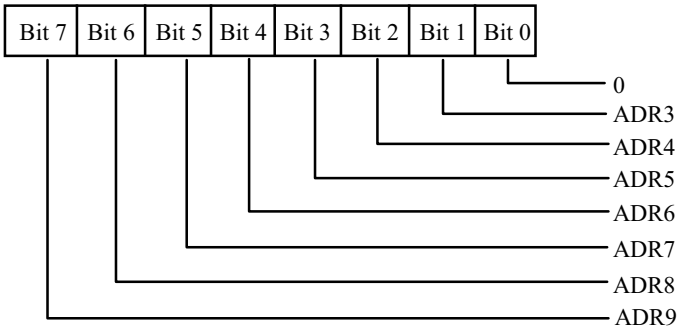
Index = C7



This register is used to select the base address of the UART1.
The serial port can be set to 96 locations on 8 byte boundaries from 100H-3F8H.
Upper address decode requirements : CS = ??and A10 =??are required to access UART 1 registers.
A[3:0] are decoded as 0xxxb

3.1.9 Second Serial port base address Register (FSR)

Index = C8



This register is used to select the base address of the UART2.
The serial port can be set to 96 locations on 8 byte boundaries from 100H-3F8H.
Upper address decode requirements : CS = ??and A10 =??are required to access UART 2 registers.
A[3:0] are decoded as 0xxxb

3.1.10 DMA Selection Register (DSR)

Index = C9

Bit 7	Bit 6	Bit 5	Bit 4	FDC DMA
0	0	0	0	None
0	0	0	1	DMA_A
0	0	1	0	DMA_B
0	0	1	1	DMA_C

Bit 3	Bit 2	Bit 1	Bit 0	Parallel DMA
0	0	0	0	None
0	0	0	1	DMA_A
0	0	1	0	DMA_B
0	0	1	1	DMA_C

This register is used to select the DMA for the FDC (bits 7:4) and the parallel port (bits 3:0). Any unselected DMA ACK output is in tristate.

3.1.11 IRQ Selection Register (IRR)

Index = CA

Bit 7	Bit 6	Bit 5	Bit 4	FDC IRQ
0	0	0	0	None
0	0	0	1	IRQ_A
0	0	1	0	IRQ_B
0	0	1	1	IRQ_C
0	1	0	0	IRQ_D
0	1	0	1	IRQ_E
0	1	1	0	IRQ_F
0	1	1	1	None
1	0	0	0	IRQ_H

Bit 3	Bit 2	Bit 1	Bit 0	Parallel IRQ
0	0	0	0	None
0	0	0	1	IRQ_A
0	0	1	0	IRQ_B
0	0	1	1	IRQ_C
0	1	0	0	IRQ_D
0	1	0	1	IRQ_E
0	1	1	0	IRQ_F
0	1	1	1	None
1	0	0	0	IRQ_H

This register is used to select the IRQ for the FDC (bits 7:4) and the parallel port (bits 3:0). Any unselected IRQ output (registers : IRR, SIR, IIR) is in tristate.

3.1.12 Serial IRQ selection Register (SIR)

Index = CB

Bit 7	Bit 6	Bit 5	Bit 4	Serial 1 IRQ
0	0	0	0	None
0	0	0	1	IRQ_A
0	0	1	0	IRQ_B
0	0	1	1	IRQ_C
0	1	0	0	IRQ_D
0	1	0	1	IRQ_E
0	1	1	0	IRQ_F
0	1	1	1	None
1	0	0	0	IRQ_H

Bit 3	Bit 2	Bit 1	Bit 0	Serial 2 IRQ
0	0	0	0	None
0	0	0	1	IRQ_A
0	0	1	0	IRQ_B
0	0	1	1	IRQ_C
0	1	0	0	IRQ_D
0	1	0	1	IRQ_E
0	1	1	0	IRQ_F
0	1	1	1	None
1	0	0	0	IRQ_H

This register is used to select the IRQ for serial port 1 (bits 7:4) and the serial port 2 (bits 3:0). Any unselected IRQ output (registers : IRR, SIR, IIR) is in tristate.

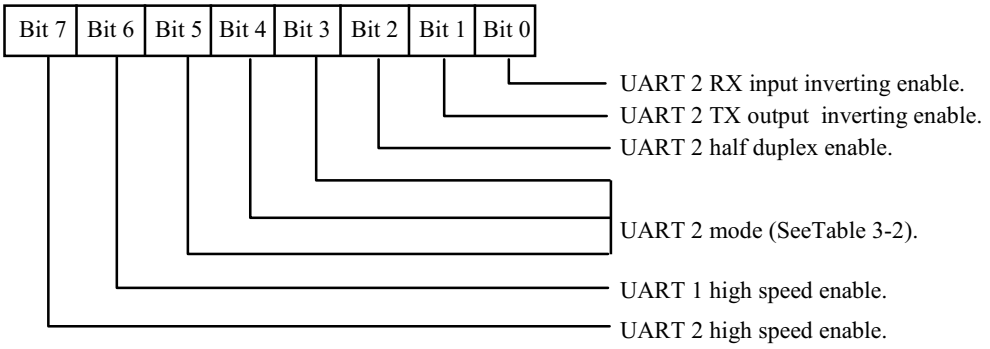
3.1.13 In IRQ selection Register (IIR)

Index = CD

This register is used to select the IRQ for IRQIN (bits 3:0), bits 7:4 are reserved and return zero when read. Any unselected IRQ output (registers : IIR, SIR, IRR) is in tristate.

3.1.14 UART Mode Register (UMR)

Index = CE



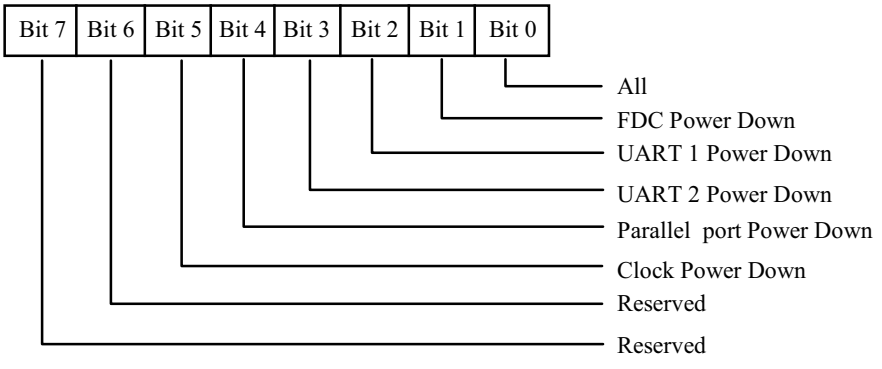
This register controls the operating mode of the UART.

Bit 5	Bit 4	Bit 3	UART 2 MODE
0	0	0	Standard (Default)
0	0	1	IrDA (HPSIR)
0	1	0	Amplitude Shift Keyed IR @ 500KHz
0	1	1	Reserved
1	x	x	Reserved

(Table 3-2. UART 2 MODE)

3.1.15 Power Down Register (PDR)

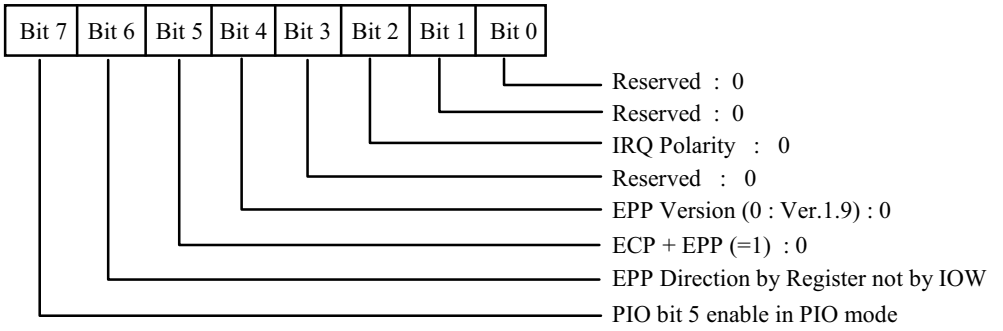
Index = CF



This register controls which part falls in power down mode.

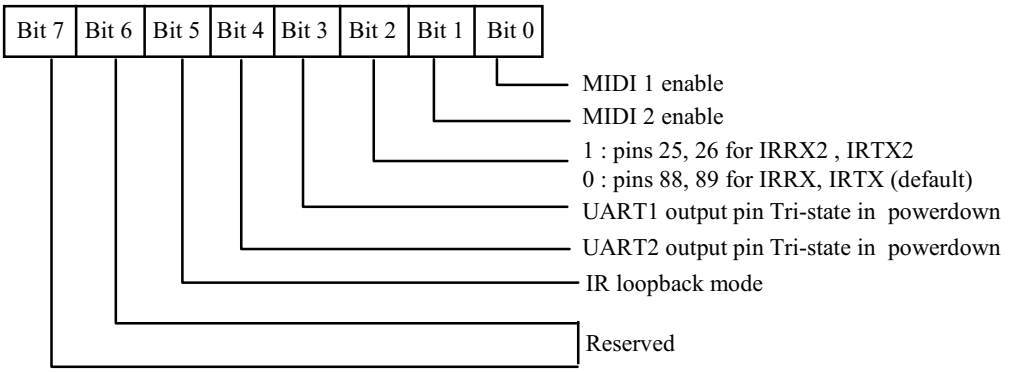
3.1.16 Printer Control Register (PCR)

Index = D0



3.1.17 MIDI Support Register (MSR)

Index = D1



MIDI enable means UART clock is 24 MHz/12 instead of 24 MHz/13

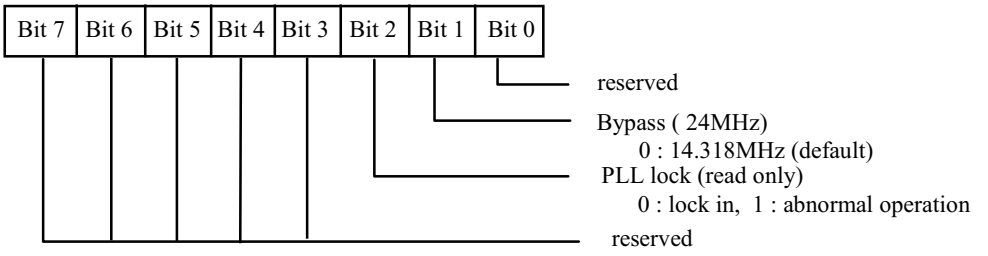
3.1.18 Test Mode Register (TMR, T3R)

Index = D2, D4

These registers are used to support chip debugging and test.
The system should not access these.

3.1.19 Clock Mode Register (T2R)

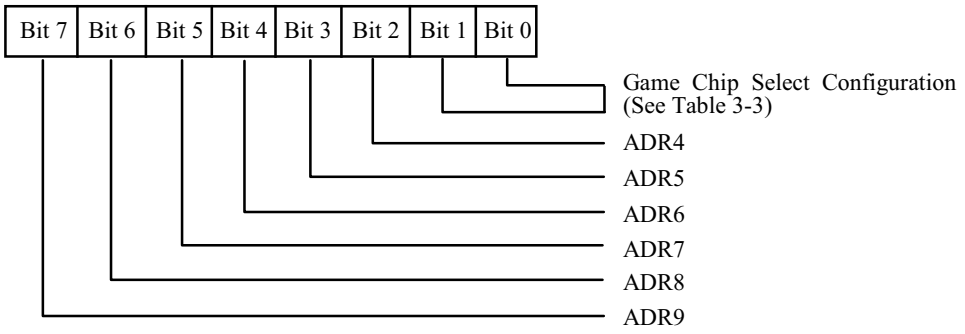
Index = D3



This register controls the operating mode of the clock generator. If you want to use 24MHz external clock, you must change bit 1 of this register . Default = 0 (14.MHz clock)

3.1.20 Game chip select Decoding Register (GDR)

Index = D5



Bit 1	Bit 0	Configuration
0	0	GAMECS Disable
0	1	ADR[3:0]= 0001b
1	0	ADR[3:0]= 0xxxb
1	1	ADR[3:0]= xxxxb

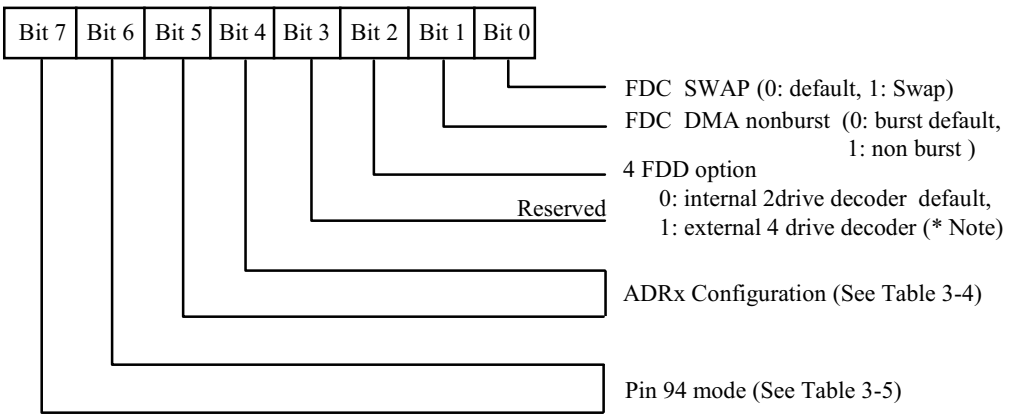
(Table 3-3. Game chip select Configuration)

Bit 5	Bit 4	Configuration
0	0	ADRx Disable
0	1	1 byte decode, ADR[3:0]= 0001b
1	0	8 byte decode, ADR[3:0]= 0xxxb
1	1	16 byte decode, ADR[3:0] = xxxxb

(Table 3-4. ADRx Configuration)

3.1.21 Pin 94 Mode Register (PMR)

Index = D6



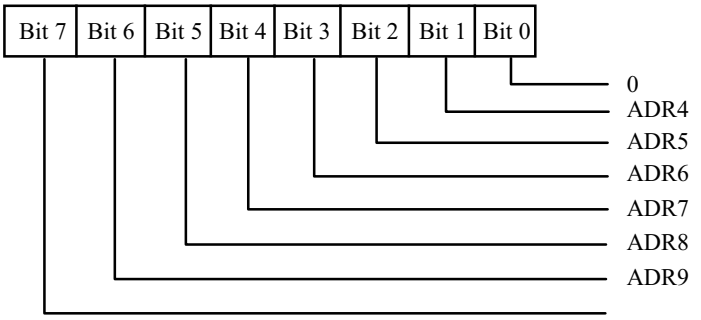
Bit 7	Bit 6	Configuration
0	x	Tri-state
1	0	ADRX
1	1	IRQ_B

(Table 3-5. Pin 94 Mode Configuration)

* Note : If you want to use 4 FDD, you require the external 2 to 4 decoder

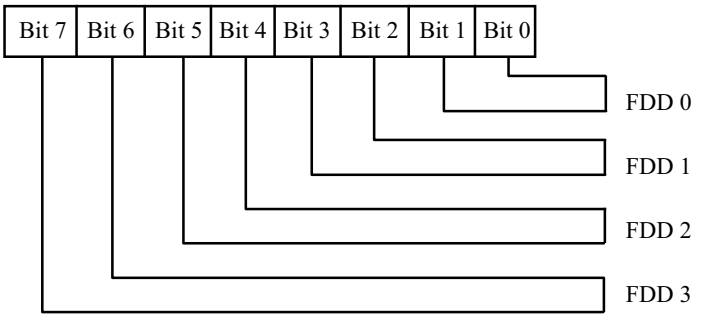
3.1.22 General purpose address Decode Register (GDR)

Index = D7



3.1.23 DRVDEN Selection Register

Index = D8



FDD 3		FDD 2		FDD 1		FDD 0	
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DT1	DT0	DT1	DT0	DT1	DT0	DT1	DT0

DTx : Drive Type Select

DT1	DT0	DRVDEN 0 (Note)	DRVDEN 1 (Note)
0	0	DENSEL	DRATE 0
0	1	DRATE 1	DRATE 0
1	0	$\overline{\text{DENSEL}}$	DRATE 0
1	1	DRATE 0	DRATE 1

Note : DENSEL, DRATE 1 and DRATE 0 map to two output pins DRVDEN0 and DRVDEN1.

3.1.19 Software Configuration procedure

Configuration is accomplished in three basic steps :

a) Enter configuration mode

b) Configure the GM82C803C

c) Escape from configuration mode

Any deviation from this sequence causes the configuration state machine to return to its initial idle state. The configuration procedure is intentionally complicated to prevent an errant program from making accidental changes to the chip configuration.

Enter Configuration Mode

Write 33h to port 398h twice consecutively.

The following is an example in 8086 assembly language:

```
MOV     DX,398h  : Port Address
MOV     AL,33h   : Data
OUT     DX, AL
OUT     DX, AL   : In configuration mode
```

Configure the Chip

The 25 configuration registers can be written to or read from.

To read or write data from/to the registers:

1. Write index to port 398h
2. Write data to port 399h/Read data from port 399h.
   (where 뱲ata?is the value to be written to/to be read from the register which the index points to.)

Before you enable any function of the chip, you should complete the function뭘 setting. (Base address, IRQ, DRQ, and etc.)

Escape from Configuration Mode

Write 55h to port 398h once.

The following is an example

```
MOV     DX, 398h      : Port Address
MOV     AL, 55h       : Data
OUT     DX, AL        : Exit from configuration mode
```

GM82C803C Configuration Registers

Index	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
C0	3C	Device ID (3C)							
C1	00	Revision number (00)							
C2	03	GCS/ PWRGDS	Reserved	IDE	FDC	UART2	UART1	PIO 1	PIO 2
C3	3C	FDC Address ADR[9:4]						0	0
C4	3C	IDE Base Address ADR[9:4]						0	0
C5	3D	IDE Status Address ADR[9:4]						0	1
C6	00	Parallel port Base Address ADR[9:2]							
C7	00	First Serial port Base Address ADR[9:3]							0
C8	00	Second Serial port Base Address ADR[9:3]							0
C9	00	FDC DRQ				Parallel port DRQ			
CA	00	FDC IRQ				Parallel port IRQ			
CB	00	Serial 1 IRQ				Serial 2 IRQ			
CC	00	Reserved							
CD	00	Reserved				IRQ IN IRQ			
CE	00	UART2 Speed	UART1 Speed	UART2 Mode			UART2 Duplex	UART2 XMIT Polarity	UART2 RCV Polarity
CF	00	Reserved		Power Down mode					
D0	00	ECP Mode						Reserved	
D1	00	Reserved			UART 1,2 mode		ALT I/O	MIDI 2	MIDI 1
D2	00	Test Mode register 1							
D3	00	Reserved					PLL lock	Bypass	Reserved
D4	00	Test Mode register 3							
D5	3C	GAME CS ADR[9:4]						GAME CS Config.	
D6	00	ADRx-IRQ_B		ADRx Config		Reserved	FDC mode		
D7	00	General Purpose Address ADR[10:4]							0
D8	00	FDD 3 -DTx		FDD 2 -DTx		FDD 1-DTx		FDD 0 -DTx	

4. FUNCTIONAL DESCRIPTION

4.1 PARALLEL PORT

The Prime 3C supports the IBM XT/AT Compatible parallel port, the PS/2 type bi-directional parallel port, the EPP (Enhanced Parallel Port) and the ECP (Extended Capabilities Port) modes. The information on selecting the mode of operation, changing base address of parallel port, powerdown parallel port and disabling parallel port are descripted at PRIME3C configuration registers.

IBM XT/AT Compatible Mode

The IBM XT/AT Compatible parallel port is selected in FSR register and supports Centronics style standard mode. The PRIME3C also supports the optional PS/2 type bi-directional parallel port by setting the bit7 of PCR register.

The registers used in compatible mode are shown in table 4-1.

REGISTER	ADDRESS
DATA (DTR)	BASE ADDRESS + 00H
STATUS (STR)	BASE ADDRESS + 01H
CONTROL (CTR)	BASE ADDRESS + 02H

(Table 4-1 Compatible Mode Register Set)

DATA REGISTER (DTR)

This register transfers 8 bit data and is located at an offset of 00H from base address. The reset value is 00H. In compatible mode, the data written to this register is transmitted to parallel port. The read operation in this mode causes the data register to present the last data written to it by CPU. In PS/2 style bi-direction mode, a write operation causes the data to be latched. If the direction bit(the bit5 of CTR) is 0, the latched data is presented on parallel port. If the direction bit is 1, the data is only latched. When direction bit is 0, a read operation in this mode causes the data register to present the last data written to port by CPU. When direction bit is 1 and bi-directional mode, a read operation causes the data on parallel port to be presented on system data port. The table 4-2 shows these operations.

MODE	DIRECTION	nIOR	nIOW	RESULT
compatible	X	1	0	DATA Written to PD[0:7]
compatible	X	0	1	DATA Read from the Output Latch
bi-direction	0	1	0	DATA Written to PD[0:7]
bi-direction	1	1	0	DATA Written is Latched
bi-direction	0	0	1	DATA Read from the Output Latch
bi-direction	1	0	1	DATA Read from PD[0:7]

(Table 4-2 Read and Write of Data Register in Compatible and Bi-direction Mode)

STATUS REGISTER (STR)

This register is located at an offset of 01H from base address and is read-only register. This register can be accessed in all parallel port modes. The bits of STR are defined as follows:

BIT 0 TIMEOUT

This bit is valid in only EPP mode and indicates that a 10 usec timeout has occurred. A logic 0 means that no timeout error has occurred. A logic 1 indicates that a timeout error has been detected. This bit can be cleared by RESET or writing a 1 to this bit. In not EPP mode, this bit is always 0.

BIT 1, 2

These bits are reserved and always 0.

BIT 3 $\overline{\text{ERROR}}$

This bit reflects the state of the $\overline{\text{ERROR}}$ input pin. A logic 0 means that error has been detected.

BIT 4 SLCT

This bit reflects the state of the SLCT input pin. A logic 1 indicates that printer is on-line. A logic 0 means printer is not selected.

BIT 5 PE

This bit reflects the state of the PE input pin. A logic 1 indicates that printer is out of paper.

BIT 6 $\overline{\text{ACK}}$

This bit reflects the state of the $\overline{\text{ACK}}$ input pin. A logic 0 indicates that printer has been received a character and is ready to accept another.

BIT 7 $\overline{\text{BUSY}}$

This bit reflects the inverted state of the BUSY input pin. A logic 0 indicates that printer is busy and cannot accept a new data.

CONTROL REGISTER (CTR)

This register is located at an offset of 02H from base address. The reset value is 00H. This read/write register provides control of all output signals. This register can be accessed in all parallel port.

BIT 0 STROBE

This bit is inverted of the $\overline{\text{STROBE}}$ pin and controls data strobe to printer.

BIT 1 AUTOFD

This bit is inverted of the $\overline{\text{AUTOFD}}$ pin. A logic 1 causes the printer to generate an automatic line feed at the end of each line.

BIT 2 $\overline{\text{INIT}}$

This bit controls INIT pin used to initialize the printer. A logic 0 generates active low pulse to initialize the printer.

BIT 3 SLCTIN

This bit is inverted of the $\overline{\text{SLCTIN}}$ pin. A logic 1 causes the printer to be selected.

BIT 4 IRQEN

This is the interrupt request enabling bit. When this bit is 1, parallel port interrupt is generated in respond to a transition of ACK signal from the printer. Otherwise, all interrupts are disabled and all pending interrupts are cleared.

BIT 5 DIR

This bit controls the parallel port direction. A logic 0 indicates that the parallel port is in output mode and a logic 1 indicates that parallel port is in input mode. In the compatible mode, this bit is always 0 regardless of the state of this bit.

BIT 6,7

These bits are reserved and always 0.

3.2 EPP MODE

The EPP mode is high speed and bi-direction protocol and the data rate is up to 2M byte/sec. The EPP mode provides for greater throughput than compatible mode by supporting faster transfer time and a mechanism that allows the host to address peripheral device registers directly. The PRIME3C supports EPP mode(IEEE 1284) that can be selected through the FSR. When PRIME3C is in EPP mode, the PRIME3C also supports PS/2 style bi-direction mode. The PRIME3C supports 2 EPP modes: EPP ver. 1.7 and ver. 1.9. The EPP version is selected by the bit 4 of PCR and the default version is ver. 1.9. There are 4 operations in EPP mode: address write, address read, data write and data read. Before accessing the EPP registers, the software must write 0's to bit0,1,3 and 5 of CTR because the output pins and direction of data are controlled by EPP hardware. If the bit 6 of PCR is 1, the software must control direction of data by setting and resetting the bit5 of CTR(direction bit). The EPP operations are closely related with the system timing(I/O read and write). For this reason, a timer is required to prevent system from being locked up. If more than 10 usec have elapsed from start of the EPP cycle, the timeout timer generates timeout error and sets the timeout bit of STR. This timeout condition is available only in EPP ver. 1.9.

The EPP mode has 8 addressable ports. These ports are defined as follows.

data port	base address + 00H	EPP data port 0	base address + 04H
status port	base address + 01H	EPP data port 1	base address + 05H
control port	base address + 02H	EPP data port 2	base address + 06H
EPP address port	base address + 03H	EPP data port 3	base address + 07H

DATA REGISTER (base address + 00H)

This register is Compatible parallel port and same with DTR register in Compatible mode.

STATUS REGISTER (base address + 01H)

This register is same with STR register in Compatible mode.

CONTROL REGISTER (base address + 02H)

This register is same with CTR register in Compatible mode.

EPP ADDRESS REGISTER (base address + 03H)

This register is cleared at initialization by RESET. A write operation to this port initiates an EPP ADDRESS WRITE operation that is used for EPP device/register selection. A read operation to this port generates EPP ADDRESS READ operation.

EPP DATA PORT 0 REGISTER (base address + 04H)

This register is cleared at initialization by RESET. Access to this port initiate EPP DATA WRITE or EPP DATA READ operations with bit[7:0].

EPP DATA PORT 1 REGISTER (base address + 05H)

This register is cleared at initialization by RESET. Refer to EPP DATA PORT 0 for a description of operation.

EPP DATA PORT 2 REGISTER (base address + 06H)

This register is cleared at initialization by RESET. Refer to EPP DATA PORT 0 for a description of operation.

EPP DATA PORT 3 REGISTER (base address + 07H)

This register is cleared at initialization by RESET. Refer to EPP DATA PORT 0 for a description of operation.

TABLE4-3. Parallel Port Pin Out

Connector Pin No.	SPP , ECP Mode	Pin Direction	EPP Mode	Pin Direction
1	STROBE	I / O	WRITE	I / O
2	PD0	I / O	PD0	I / O
3	PD1	I / O	PD1	I / O
4	PD2	I / O	PD2	I / O
5	PD3	I / O	PD3	I / O
6	PD4	I / O	PD4	I / O
7	PD5	I / O	PD5	I / O
8	PD6	I / O	PD6	I / O
9	PD7	I / O	PD7	I / O
10	ACK	I	ACK	I
11	BUSY	I	WAIT	I
12	PE	I	PE	I
13	SLCT	I	SLCT	I
14	AUTOFD	I / O	DSTRB	I / O
15	ERROR	I	ERROR	I
16	INIT	I / O	INIT	I / O
17	SLCTIN	I / O	ASTRB	I / O

ECP MODE

The ECP mode is another high -speed bi-directional protocol that is implemented in hardware to reduce software and system overhead.
The ECP mode provided DMA operation, a 16-byte FIFO, bi-directional command/data transfer, command/data FIFO tag (one per byte), a FIFO threshold interrupt for both directions, FIFO full and full status bits, automatic generation of strobes by hardware to fill or empty the FIFO and a Run Length Encoding(RLE). The ECP mode is selected in Function Selection Register(FSR). Once selected, its mode is controlled via the mode field of bit 5,6,7 of ECR Register. The ECP mode in Prime3C has 10 registers and these registers are shown in **table 4.4**.

Register definition

The register definition are based on the standard printer address for LPT. All of standard modes are supported in ECP mode. The port register varies depending on the mode field in the ECR. The **table 4.4** lists these dependencies.

Table 4-4. ECP Register Definitions

Register	Address	R/W	Mode	Index
data	Base addr + 000h	R/W	000-001	data register
ecpAfifo	Base addr + 000h	R/W	011	ECP FIFO(Address)
dsr	Base addr + 001h	R/W	ALL	status register
dcr	Base addr + 002h	R/W	ALL	control register
cFIFO	Base addr + 400h	R/W	010	parallel port data FIFO
ecpDfifo	Base addr + 400h	R/W	011	ECP FIFO (DATA)
tFIFO	Base addr + 400h	R/W	110	TEST FIFO
cnfgA	Base addr + 400h	R	111	configuration register A
cnfgB	Base addr + 401h	R/W	111	configuration register B
ecr	Base addr + 402h	R/W	ALL	extended control register

data (0x000 Modes 000,001 : Parallel Port Data Register)

This is the standard parallel port data register. Writing to this register in mode 000 shall drive data to the parallel port data lines. In all other modes the drivers may be tri-stated by setting the direction bit in the **dcr**. Read to this register return the value on the data lines.

ecpAFifo (0x000 Modes 011 : ECP FIFO - Address/ RLE)

A data byte written to these address is placed in the FIFO and tagged as a ECP Address / RLE. The gardware at the ECP port will transmit this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (**direction** is 0).

Table. ECP Address FIFO

<7>	W	Indicates data Type
	1:	Bit <6:0> are a ECP Address
	0:	Bit field <6:0> is a run length, indicating how many times the next data byte is to appear (0 = 1 time, 1 = 2 times, 2 = 3 times, etc.).
<6:0>	W	Address or RLE field described above.

dsr (0x001 : Device Status Register)

This read-only register reflects the inputs on the parallel port interface.

Table. Device Status Register

<7>	R	$\overline{\text{Busy}}$	inverted version of parallel port **Busy** signal.
<6>	R	$\overline{\text{Ack}}$	version of parallel port $\overline{\textbf{Ack}}$ signal.
<5>	R	Error	version of parallel port **Error** signal.
<4>	R	Select	version of parallel port **Select** signal.
<3>	R	$\overline{\text{Fault}}$	version of parallel port $\overline{\textbf{Fault}}$ signal.
<2:0>	R	reserved	returns undefined when read.

dcr (0x002 : Device Control Register)

This register directly controls several output signals as well as enabling some functions. The drivers for $\overline{\text{Strobe}}$, $\overline{\text{AutoFd}}$, $\overline{\text{Init}}$, and $\overline{\text{SelectIn}}$ are open-collector in mode 000, and are push-pull in all other modes.

Table. Device Control Register

<7:6>	R	Reserved, returns undefined when read.
<5>	R/W	Direction
	1:	If mode = 000 or mode = 010, we are standard parallel port and this bit has no effect (drivers are enabled). Otherwise, this bit tri-states the drivers and sets the direction so that data will be read from the peripheral.
	0:	Drivers are enabled. DMA, data are written to the peripheral.
<4>	R/W	ackIntEn
	1:	Enables an interrupt on the rising edge of $\overline{\text{Ack}}$.
	0:	Disables the $\overline{\text{Ack}}$ interrupt.
<3>	R/W	SelectIn is inverted and then driven as parallel port $\overline{\text{SelectIn}}$.
<2>	R/W	$\overline{\text{Init}}$ is driven as parallel port $\overline{\text{Init}}$.
<1>	R/W	AutoFd is inverted and then driven as parallel port $\overline{\text{AutoFd}}$.
<0>	R/W	Strobe is inverted and then driven as parallel port $\overline{\text{Strobe}}$.

cFifo (0x400 , Mode = 010 : Parallel Port Data FIFO)

Data written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are PWord aligned. If odd bytes need to be transferred then the operation must be handled in mode 000. This mode is only defined for the forward direction.

ecpDFifo (0x400 , Mode = 011 : ECP Data FIFO)

Data written or DMAed from the system to these FIFO when direction is 0 are transmitted to the peripheral by hardware handshake using the ECP parallel port protocol, Transfers to the FIFO are PWord-aligned. Ifodd bytes need to be transferred then the operation must be handled in mode 000.

Data from the peripheral are read under automatic hardware handshake from ECP into this FIFO when direction is 1. Reads or DMAs from the FIFO will return ECP data to the system.

tFifo (0x400 mode 110)

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.
Data in the tFIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port lines.
The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data into a full tFIFO, the new data is not accept into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read.
The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance merits.
The FIFO size and the interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.
The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntr Threshold can be determined by setting the direction bit to 1 and filling the empty tFIFO with a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached. Data bytes are always read from the head of tFIFO regardless of the values of the direction bit. For example, if 44h, 33h, 22h are written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as they were written.

cnfgA (0x400 mode 111)

This configuration register is read only register. When read, 10h is returned. This indicates to the system that this is an 8-bit implementation.

cnfgB (0x401 mode 111)

This configuration register is read only register.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0		0	0	0	0	0	0

→ This bit returns the values on the ISA IRQ line to determine the possible conflicts.

ecr (0x402 mode all)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

→ **Empty** : Read only
1: The FIFO is completely empty
0: The FIFO contains at least 1 byte of data.

→ **Full** : Read only
1: The FIFO cannot accept another byte or the FIFO is completely full
0: The FIFO has at least 1 free byte.

→ **Service Intr** : Read/Write
1: Disables DMA and all of the service interrupts
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred, serviceIntr bit shall be set to 1 by hardware, and it must be reset to 0 to re-enable the interrupts.
case dmaEn =1:
During DMA (this bit is set to 1 when terminal count is reached).
case dmaEn =0 direction = 0:
This bit shall be set to 1 whenever there are writeIntrThreshold or more free in FIFO
case dmaEn =0 direction =1:
This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to the read from the FIFO.

→ **DMA En** : Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

→ **$\overline{\text{Err Intr En}}$** : Read/Write (Valid only in ECP mode)
1: Disables the interrupt generated on the asserting edge of $\overline{\text{nFault}}$
0: Enables an interrupt pulse on the high to low edge of $\overline{\text{Fault}}$. Note that an interrupt will be generated if $\overline{\text{Fault}}$ is asserted (interrupting) and this bit is written from 1 to 0. This prevents interrupt from being lost in the time between the read of the ECR and the write of the ECR.

→ These bits are Read/Write and select the Mode. See the table 4-5.

Table 4-5. Mode description.

Mode	Description
000:	*Standard Parallel Port mode.* In this mode the FIFO is reset and common collector drivers are used on the control lines (Strobe, AutoFd, Init and SelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	*PS/2 Parallel Port mode.* Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. It is always best for the hardware design to read the value of the lines and not the register, some old Centronics interfaces actually returned the reg. value and not the wire value. All drivers have active pull-ups (push-pull).
010:	*Parallel port FIFO mode.* This is the same as 000 except that PWords are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	*ECP Parallel port mode.* In the forward direction (direction is 0) PWords placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into PWords in the ecpDFifo. All drivers have active active pull-ups (push-pull).
100:	*EPP mode.* (If this option is enabled in the configuration register)
101:	Reserved.
110:	*Test mode.* In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port.
111:	*Configuration mode.* In this mode the confgA, confgB registers are accessible at 0x400 and 0x401.

OPERATION

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and ECP port only in the data transfer phase (mode 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.
If the port is in mode 000 or 001, it may switch to any other mode. If the port is not in mode 000 or 001, it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode, the software should wait for the FIFO to be empty before switching back to the mode 000 or 001. In this case, all control signals will be deasserted before the mode switch. In an ECP reverse mode, the software waits for all the data to be read from the FIFO before changing back to the mode 000 or 001. Since the automatic hardware ECP reverse handshake only cares about the state of the FIFO, it may have acquired extra data which will be discarded. It may, if fact, be in the middle of a transfer when the mode is changed back to 000 or 001. In this case, the port will desert AutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

Command/Data

ECP mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit data or 8-bit commands.
In the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low.
The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.
In the reverse direction , normal data is transferred when PeriphAck is high and 8-bit command is transferred when PeriphAck is low. The most significant bit of command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 4-6. Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D (6:0)
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

Data Compression

Prime3C supports Run Length Encoded (RLE) decompression in hardware and can transfer compressed data to the peripheral. Run Length Encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count in written to the ecpAfifo and the data byte is written to the ecpDFifo. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition

The drivers $\overline{\text{STROBE}}$, $\overline{\text{AutoFd}}$, $\overline{\text{Init}}$ and $\overline{\text{SelectIn}}$ are open-collector in mode 000 and are push-pull in all other modes.

ISA Connections

The interface can never stall causing the host to hang. The width of data transfer is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. Single byte wide transfers.

DMA Transfer

DMA transfers are always to or from the ecpDfifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests, dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting PDACK and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more then 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until PDACK is deasserted for a minimum of 350nsec. (Note : The dnly way to properly terminate DMA transfers with a TC)
DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting service Intr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode-Transfers from the FIFO to the Host

(Note : In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the Parallel DRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the Parallel DRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by Parallel $\overline{\text{DACK}}$) indicating that no more data is required. Parallel DRQ goes inactive after Parallel $\overline{\text{DACK}}$ goes active for the last byte of a data transfer (or on the active edge of IOR, on the last byte, if no edge is present on Parallel $\overline{\text{DACK}}$. If Parallel DRQ goes inactive due to the FIFO going empty, then Parallel DRQ is active again as soon as there is one byte in the FIFO. If Parallel DRQ goes inactive due to the TC, then Parallel DRQ is active again when there is one byte in the FIFO and serviceIntr has been re-enabled. (Note : A data underrun may occur if Parallel DRQ is not removed in time to prevent an unwanted cycle.)

Interrupt

The interrupts are enabled by serviceIntr in the ECR register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from 1 to 0. This can occur during programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.

An interrupt is generated when :

1. For DMA transfer : When serviceIntr is 0,dmaEn is 1 and the DMA TC is received.

2. For Programmed I/O :
   a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.

   b. When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.

3. When $\overline{\text{ErrIntrEn}}$ is 0 and $\overline{\text{Fault}}$ transitions from high to low or when $\overline{\text{ErrIntEn}}$ is set from 1 to 0 and Fault is asserted.

4. When ackIntrEn is 1 and the Ack signal transitions from low to high.

FIFO Operation

The FIFO threshold is fixed by 8 and supported only in mode 010 and 011. Each data byte is transferred to FIFO by PIO cycle or DMA. Automatic data transfer is achieved using FIFO.

Programmed I/O MODE or NON-DMA MODE

The ECP or Fast Centronics mode may also be operated using interrupt driven programmed I/O. In Prime3C WriteIntrThreshold and ReadIntrThreshold are fixed to 8 bytes.
Programmed I/O transfer are to the ecpDFIFO and ecpAFIFO or from ecpDFIFO, or to/from the tFIFO. To use the PIO transfers, the host first sets up direction and state and sets dmaEn to 0 and serviceIntr to 0. The ECP requests PIO transfers from the host by activating the PINTR pin. The PIO will empty or fill the FIFO using appropriate direction and mode.

Transfer from the HOST to the FIFO

In the forward direction, an interrupt occurs when service interrupt is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty, it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with WriteIntrThreshold byte. If an interrupt occurs, the host must respond to therequest by writing data to the FIFO.

Transfer from the FIFO to the HOST

In the backward direction, an interrupt occurs when service interrupt is 0 and there are readIntrThreshold or more bytes are available in the FIFO. At this time if the FIFO is full, it can be emptied completely in a single burst. Otherwise it may be filled with WriteIntrThreshold bytes. If an interrupt occurs, the host must respond to the request by reading data from the FIFO.

ECP FORWARD (WRITE) OPERATION

1. An ECP write cycle starts when the ECP drives the popped tag onto $\overline{\text{AFD}}$ and the popped byte onto PD<7:0>.
2. When BUSY is low, the ECP asserts $\overline{\text{STROBE}}$ and waits for BUSY to be high.
3. When BUSY is high, the ECP deasserts $\overline{\text{STROBE}}$.
4. The ECP may change $\overline{\text{AFD}}$ and PD<7:0> in preparation for next cycle when BUSY is low.

ECP BACKWARD (READ) OPERATION

1. An ECP read cycle starts when the ECP drives $\overline{\text{AFD}}$ low.
2. The peripheral device drives BUSY high for a normal data read cycle, or drives BUSY low for a command read cycle and drives the byte to be read onto PD<7:0>.
3. When $\overline{\text{ACK}}$ is asserted, the ECP reads the PD<7:0> and drives $\overline{\text{AFD}}$ high.
4. When $\overline{\text{AFD}}$ is high, the peripheral device deasserts $\overline{\text{ACK}}$ and may change BUSY and PD<7:0> in preparation for the next cycle.

The FDC contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. The FDC is capable of supporting either IBM3740 single density format(FM), or IBM system 34 double density format (MFM) including double sided recording. It simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface. It supports data rates of 250/300/500 Kb/s and 1Mb/s. This block integrates ; Formatter/ Controller, Data Seperation,Write Precompensation,Data Rate Selection,Clock Generation, Drive interface drivers and receivers. It has five registers which may be accessed by the main system processor; a Main Status Register(MSR), a Data rate Selection Register(DSR), a Data Register(DR), a Control Register(CR), and a Operation Register(OR). The main status register contains the status information of the FDC, and may be accessed at any time. The data rate selection register is used to program the data rate, amount of write precompensation, power down mode, and software reset. The data register (actually consists of several registers in a stack with only one register presented to the data bus at a time) stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into the data register in order to program or obtain the results after execution of a command. The status register may only be read and is used to facilitate the transfer of data between the processor and FDC.

Table 4-7. Register Description and Address

FDC Base Address (Hex)	R/W	Register
+ 0		Reserved
+ 1		Reserved
+ 2	R/W	Operation Register (OR)
+ 3		Reserved
+ 4	R	Main Status Register (MSR)
+ 4	W	Data Rate Select Register (DSR)
+ 5	R/W	Data Register(FIFO) (DR)
+ 6		Reserved
+ 7	W	Control Register (CR)
+ 7	R	Read DSKCHG (D7 only, inverse)

FIFO (Data Register)

The FIFO is used to transfer disk data. It is 16 bytes in size and has programmable threshold values. Data transfers are governed by the RQM and DIO bits in the Main Status Register.
The FIFO has the defaults with 765B compatible mode after a hardware reset. Software resets (Reset via OR or DSR Register) can also place the FDC into 765B compatible mode if the LOCK bit is set to zero(See the definition of the LOCK bit in Lock command). This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 4-8 gives several examples of the delays with a FIFO. The data is based upon the following formula.

$$\text{Threshold\#} \times \left| \frac{1}{\text{Data Rate}} \times 8 \right| - 1.5\mu s = \text{Delay}$$

Table 4-8. FIFO Service Delay

FIFO Threshold Example	Maximum Delay to Servicing at 1 Mbps Data Rate
1 byte	$1 \times 8\ \mu s - 1.5\ \mu s = 6.5\ \mu s$
2 byte	$2 \times 8\ \mu s - 1.5\ \mu s = 14.5\ \mu s$

FIFO Threshold Example	Maximum Delay to Servicing at 500 Kbps Data Rate
1 byte	$1\times16\mu s - 1.5\ \mu s = 14.5\ \mu s$
2 byte	$2\times16\mu s - 1.5\ \mu s = 30.5\ \mu s$
8 byte	$8\times16\mu s - 1.5\ \mu s = 126.5\ \mu s$
15 byte	$15\times16\mu s - 1.5\ \mu s = 238.5\mu s$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data is not transferred. An overrun or underrun will terminate the current command and the transfer of data. Disk Write will complete the current sector by generating a 00H pattern and valid CRC.

Main Status Register (MSR)

MSR indicates the current status of the disk controller. It is always available to be read and controls the flow of data to and from the Data Register (FIFO).

Table 4-10 Main Status Register

Bit	Symbol	Name	Function
D7	RQM	Request for Master	Indicates that host can access the Data Register if one. No access should be attempt if zero.
D6	DIO	Data In/Out	Indicates the direction of the data transfer only when RQM is one. If one, transfer is from Data Register to host. If zero, transfer is from host to Data Register.
D5	EXM	Execution Mode	This bit is set to one only during execution phase in Non-DMA mode. When zero, execution phase has ended and result phase has started. EXM remains 0 if DMA mode is selected.
D4	CB	Controller Busy	A Read or Write is in progress. FDC will not accept any other command.
D3	F3B	FDD 3 Busy	If one, FDD number 3 is in seek mode. It will not accept Read or Write Command. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive..
D2	F2B	FDD2 Busy	Same as above for FDD2.
D1	F1B	FDD1 Busy	Same as above for FDD1.
D0	F0B	FDD0 Busy	Same as above for FDD0.

Result Phase Status Register (ST0, ST1, ST2, ST3)

The result phase of a command contains bytes that hold status information. The four result phase status registers are read from the Data Register only during the result phase of certain commands. Those may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

Table 4-11. Status Register 0 (ST0)

Bit	Symbol	Name	Function
7,6	IC	Interrupt Code	00 : Normal termination of command was completed and properly executed. 01 : Abnormal termination of command. Execution of command was started but was not successfully completed. 10 : Invalid command issue. Command which was issued was never started. 11 : Internal drive ready status changed state during the drive polling mode. Only occurs after a reset.
5	SE	Seek End	When the FDC completes the Seek command, this flag is set to 1.
4	EC	Equipment Check	If Track 0 signal fails to occur after 255 step pulses (Recalibrate command), then this flag is set to 1.
3		Unused	Always 0.
2	HS	Head Select	Indicates the HDSEL (pin# : 11) status.
1,0	DS1,0	Drive Select 1,0	Indicates the logical drive status selected. 00 : Drive 0, 01 : Drive1 10 : Drive 2, 11 : Drive3

Table 4-12. Status Register 1 (ST1)

Bit	Symbol	Name	Function
7	EN	End of cylinder	The FDC tried to access a sector beyond the final sector of a cylinder. It will be set if TC is not issued after Read or Write Data command.
6		Unused	Always 0.
5	DE	Data Error	When the FDC detects a CRC error in either ID field or data field, this flag is 1.
4	OR	Overrun	If the FDC is serviced by host during data transfers within a certain timer interval, this flag is 1.
3		Unused	Always 0.
2	ND	No Data	Any one of the following : 1. During Read (Deleted) Data command, FDC do not find the specified sector. 2. During Read ID command , FDC cannot read the ID field without an error. 3. During Read a Track command, the FDC can not find the proper sector sequence.
1	NW	Not Writable	During Write (Deleted) Data or Format a Track command, if FDC detects a WRTPRT (pin#:14) signal from the FDD, then this flag is 1.
0	MA	Missing Address Mark	Any one of the following : 1. The FDC do not detect an ID address mark at the specified track after encountering the index hole pulse twice. 2. The FDC can not detect a data address mark or a deleted data address mark on the specified track.

Table 4-13. Status Register 2 (ST2)

Bit	Symbol	Name	Function
7		Unused	Always 0.
6	CM	Control Mark	Any one of the following : 1. During Read Data command, the FDC encounters a deleted data address mark. 2. During Read Deleted Data command , the FDC encounters a data address mark.
5	DE	Data Error	The FDC detect a CRC error in data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3	SE	Scan Equal	During Scan command, the Equal condition satisfied.
2	SN	Scan Not	During Scan command, the FDC cannot find a sector on the cylinder which meets the desired condition.
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF(hex) which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MA	Missing Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 4-14. Status Register 3 (ST3)

Bit	Symbol	Name	Function
7		Unused	Always 0.
6	WP	Write Protected	Indicates the status of the $\overline{\text{WRTPRT}}$ pin.
5		Unused	Always 1.
4	TO	Track 0	Indicates the status of the $\overline{\text{TRK00}}$ pin.
3	WP	Write Protected	Same as Bit 6.
2	HS	Head Select	Same as Bit 2 of ST0.
1,0	DS1,0	Drive Select 1,0	Same as Bit 1,0 of ST0.

Data Rate Select Register (DSR)

This write-only register is used to program the timings of the drive control signals. To ensure that drive timings are not violated when changing data rates, choose a drive timing such that the fastest data rate will not violate the timing. The data rate is programmed via the Control Register, not the DSR. Other application can set the data rate in the DSR. The data rate of the floppy controller is determined by the most recent write to either the DSR or CR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which correspond to the default precompensation setting and 250 Kbps.

D7 Software Reset : This bit behaves the same as Operations Register RESET except that this reset is self clearing.

D6 Power Down : This bit will put the controller into the Manual Low Power mode when set to one.

D5 Undefined. Should be set to zero.

D4-2 Precompensation Select : These three bits select the amount of write precompensation which the floppy controller will use on the WDATA disk interface output. Table 4-15 shows the amount of precompensation used for each bit pattern. In most cases, the default values (Table 4-16) can be used ; however, alternate values can be chosen for specific types of drives and media. Track 0 is the default starting track number can be changed in the Configure command.

Table 4-15. Write Precompensation Delays

Precomp. 4 3 2	Precompensation Delays
1 1 1	0.0 ns — Disabled
0 0 1	41.7 ns
0 1 0	83.3 ns
0 1 1	125.0 ns
1 0 0	166.7 ns
1 0 1	208.3 ns
1 1 0	250.0 ns
0 0 0	Default

Table 4-16. Default Precompensation Delays

Data Rate	Precompensation Delays
1 Mbps	41.7 ns
500 Kbps	125.0 ns
300 Kbps	125.0 ns
250 Kbps	125.0 ns

D1-0 Data Rate Select 1,0 : These bits determine the data rate for the floppy controller. See Table 4-17 for the corresponding data rate for each value of D1, D0. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

Table 4-17. Data Rates

Data Rate Select		Data Rate	
1	0	MFM	FM
1	1	1 Mbps	Illegal
0	0	500 Kbps	250 Kbps
0	1	300 Kbps	150 Kbps
1	0	250 Kbps	125 Kbps

Control Register (CR)

This register sets the data rate and is write only. This is not affect by a software reset, and is set to 250 Kbps after a hardware reset. The data rate of the floppy disk controller is determined by the last write to either this register or DSR.

D7-2 Reserved : Should be set to 0.

D1-0 Data Rate Select 1,0 : See Table 4-17 for the appropriate values.

Operation Register (OR)

This register controls the drive select and motor, enables disk interface outputs the DMA logic, and contains a software reset bit. It is set to 00H after a hardware reset, and is unaffected by a software reset.

2 Drive Select (Bit 2 of PMR is 0)

D7-6 Should be 0.
D5 Motor on enable : Inverted output $\overline{\text{MTR1}}$ (pin# : 5) is active.
D4 Motor on enable : Inverted output $\overline{\text{MTR0}}$ (pin# : 2) is active.
D3 DMA enable : Set to 1 will enable the DRQ, DACK, TC and IRQ pins.
Set to 0 will disable TC, DACK pins and make IRQ, DRQ pins Hi-Z state.
D2 Software Reset : Active low software reset signal.
D1 Should be 0.
D0 Drive Select : If 0 and D4=1, then DS0 (pin# :4) is active.
If 1 and D5=1, then DS1 (pin# :3) is active.

4 Drive Select (Bit 2 of PMR is 1)

Table 4-18. Operation Register for 4 Drive support *Note : Bits 2 and 3 are the same as 2 Drive select.

Bits						Drive Pins				Encoded Functions
7	6	5	4	1	0	DS1	DS0	MTR1	MTR0	
			1	0	0	0	0	1	0	Active Drive & Motor 0
		1		0	1	0	1	1	0	Active Drive & Motor 1
	1			1	0	1	0	1	0	Active Drive & Motor 2
1				1	1	1	1	1	0	Active Drive & Motor 3

During command or result phase, the main status register must be read by the processor before each byte of information is written into or read from the data register. Bit 6 and 7 in the main status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the FDC. Many of the commands require multiple bytes and as a result, the main status register must be read prior to each byte transfer to the FDC. On the other hand, during the result phase, bit 6 and 7 in the main status register must both be 1뭘 before reading each byte from the data register. (This result of the main status register before each byte transfer to the FDC is required only in the command and result phase, and not during the execution phase.)

During the execution phase, the main status register need not be read. If the FDC is in the Non-DMA mode, then the receipt of each data byte (if FDC is reading data form FDD) is indicated by an interrupt signal on IRQ pin. The generation of a read signal will reset the interrupt fast enough, then it may poll the main status register and then bit 7 (RQM) functions just like the interrupt signal. If a Write command is in process, then the signal performs the reset to the interrupt signal.

It is important to note that during the result phase all bytes shown in the command table must be read. The Read Data Command, for example, has seven bytes of data in the result phase. All seven bytes must be read in order to successfully complete the Read Data Command. The FDC will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the result phase.

The bytes of data which are sent to the FDC to form the command phase, and are read out of the FDC in the result phase, must occur in the order shown in the command table. That is, the command code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the command or result phase are allowed. After the last byte of data in the command phase is sent to the FDC, the execution phase automatically ended and the FDC is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to TC pin. This is a convenient means of ensuring that the processor may always get the FDC뭘 attention even if the disk system hangs up in an abnormal manner.

The FDC continues to transfer data until the TC input is active. In Non-DMA host transfers are not the normal procedure. If the user chooses to do so, the FDC will successfully complete commands, but will always give abnormal termination error status since TC is qualified by an inactive NACK. In Non-DMA mode, it is necessary to examine the main status register to determine the cause of the interrupt since it could be a data interrupt or a command termination interrupt, either normal or abnormal.

If the FDC is in the DMA mode, no interrupts are generated during the execution phase. The FDC generates DRQ's (DMA Requests) when each byte of data is available. The DMA controller responds to this request with both a DACK=0 (DMA Acknowledge) and a RD=0 (host read). If a Write Command has been programmed then a host write signal will appear instead of host read. After the execution phase has been completed (TC occurred), then an interrupt will occur (IRQ6=1). This signifies the beginning of the result phase. When the first byte of data is read during the result phase, the interrupt is automatically reset (IRQ=0).

Command Parameters

The FDC is capable of executing 23 different commands. Each command is initiated by a multibyte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases;

- Command Phase : The FDC receives all information required to perform a particular operation from the processor.
- Execution Phase : The FDC performs the operation it was instructed to do.
- Result Phase : After completion of the operation, status and other housekeeping information are made available to the processor.

Table 4 - 19 Command List

Read Data
Read Deleted Data
Write Data
Write Deleted Data
Read a Track
Read ID
Formal a Track
Scan Equal
Scan Low or Equal
Scan High or Equal
Recalibrate
Sense Interrupt Status
Specify
Sense Drivers Status
Seek
Verify
Version
Lock
Configure
Relative Seek
Dumpreg
Perpendicular Mode
Invalid

READ DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	SK	0		0	1	1	0	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

READ DELETED DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	SK	0		1	1	1	0	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

WRITE DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	0	0		0	1	1	0	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

WRITE DELETED DATA

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	0	0		1	0	0	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution. The four bytes are compared against header on floppy disk.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R					R					
	R					N					

READ A TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	MF	SK	0		0	0	1	0	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system. FDD reads all data fields from index hole of EOT
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

READ ID

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	MF	0	0		1	0	0	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
EXECUTION											The first correct ID information on the cylinder is stored in Data Register.
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

FORMAT A TRACK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	MF	0	0		1	1	0	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				N				→	Bytes/Sector
	W	←				SC				→	Sector/Track
	W	←				GPL				→	Gap 3
	W	←				D				→	Filler Byte
EXECUTION											Floppy Dik Controller (FDC) formats an entire track.
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	In this cae, the ID information has no meaning.
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

SCAN EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	SK	1		0	0	0	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

SCAN LOW OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	SK	1		1	0	0	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				STP				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

SCAN HIGH OR EQUAL

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MF	SK	1		1	1	0	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	←				C				→	Sector ID information prior to command execution.
	W	←				H				→	
	W	←				R				→	
	W	←				N				→	
	W	←				EOT				→	
	W	←				GPL				→	
	W	←				DTL				→	
EXECUTION											Data transfer between FDD and main system
RESULTS	R	←				ST0				→	Status information after command execution
	R	←				ST1				→	
	R	←				ST2				→	
	R	←				C				→	Sector ID information after command execution
	R	←				H				→	
	R	←				R				→	
	R	←				N				→	

RECALIBRATE

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		0	1	1	1	Command Codes
	W	X	X	X	X		X	0	DS1	DS0	
											Head retracted to Track zero.

SENSE INTERRUPT STATUS

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		1	0	0	0	Command Codes
	R	← STO →									Status information about the FDC at the end of seek operation.
	R	← PCN →									

SPECIFY

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		0	0	1	1	Command Codes
	W	← SRT →				← HUT →					
	W	← HLT →								ND	

SENSE DRIVE STATUS

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		0	1	0	0	Command Codes
	W	X	X	X	X		X	0	DS1	DS0	
RESULTS	R	← ST3 →									Status information about the FDC.

SEEK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		1	1	1	1	Command Codes
	W	X	X	X	X		X	HS	DS1	DS0	
	W	← NCN →									
EXECUTION											Head is positioned over proper cylinder on the diskette.

VERIFY

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	MT	MFM	SK	1		1	1	1	0	Command Codes
	W	EC	0	0	0		0	HDS	DS1	DS0	
	W	←			C					→	Sector ID information prior to command execution.
	W	←			H					→	
	W	←			R					→	
	W	←			N					→	
	W	←			EOT					→	
	W	←			GPL					→	
	W	←			STP					→	
EXECUTION											No data transfer takes place.
RESULTS	R	←			ST0					→	Status information after command execution
	R	←			ST1					→	
	R	←			ST2					→	
	R	←			C					→	Sector ID information after command execution
	R	←			H					→	
	R	←			R					→	
	R	←			N					→	

VERSION

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		0	1	0	0	Command Codes
RESULTS	R	1	0	0	1		0	0	0	0	Enhanced Controller

CONFIGURE

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	1		0	0	1	1	Configure Information
	W	0	0	0	0		0	0	0	0	
	R	0	EIS	EFIFO	POLL	←		FIFOTHR		→	
	W	←			PRETRK					→	

RELATIVE SEEK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	1	DIR	0	0		1	1	1	1	
	W	0	0	0	0		0	HDS	DS1	DS0	
	W	←			RCN					→	

DUMPREG

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		1	1	1	0	* Note
EXECUTION											Register placed in FIFO
RESULTS	R	← PCN-Drive0 →									
	R	← PCN-Drive1 →									
	R	← PCN-Drive2 →									
	R	← PCN-Drive3 →									
	R	← SRT →					← HUT →				
	R	← HUT →									
	R	← SC / EOT →									
	R	LOCK	0	D3	D2		D1	D0	GAP	WGATE	
	R	← ST0 →									

PERPENDICULAR MODE

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	0	0	0	0		0	1	0	0	Command Codes
	W	OW	0	D3	D2		D1	D0	GAP	WGATE	

LOCK

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	LOCK	0	0	1		0	1	0	0	Command Codes
RESULTS	R	0	0	0	LOCK		0	0	0	0	

INVALID

PHASE	R/W	D7	D6	D5	D4		D3	D2	D1	D0	R/W
COMMAND	W	← Invalid Codes →									Invalid Command Codes(NoOp-82077AA goes into Standby State)
RESULTS	R	← ST0 →									ST0 = 80H

PARAMETER ABBREVIATIONS

C Cylinder Number. The currently selected cylinder number 0 through 225.
D0-3 Drive Select 0-3. Designates which drives are perpendicular drives, a 1 indicating perpendicular drive.
D Data. The pattern to be written in each sector data field during formal
DIR Direction. If this bit is 0, then the head will step out from the inside during a relative seek. If set to 1, the head will step in toward inside.
DS1,0 Disk Drive Select

DS1	DS0	Disk Drive
0	0	drive 0
0	1	drive 1
1	0	drive 2
1	1	drive 3

DTL Data Length. When N is defined as 00(hex), DTL stands for the Data length which users are going to read out or write into the sector. When N is not zero, DTL has no meaning and should be set to FF(hex).
EC Enable Count. When this bit is 1, the DTL parameter of the verify command becomes SC (Number of sectors per track).
EFIFO Enable FIFO. When this bit is 0, the FIFO is enabled. A 1 pulse the FDC in the NEC765 compatible mode where the FIFO is disabled.
EIS Enable implied seek. when this bit is 1, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A 0 disables the implied seek.
EOT End of track. The final sector number on a cylinder.
GAP Alters Gap2 length when using perpendicular mode.
GPL Gap Length. The Gap3 size. During the Format command, it determines the size of Gap3.
H/HS Head Address.. It stands for head number 0 to 1, as specified in ID field.
HLT Head Load Time. The time interval that FDC waits after loading the head and before initiating a read or write operation. See specify command.
HUT Head Unload Time. The time interval from the end of the execution phase of a Read or Write command until the head is unloaded. See specify command.
Lock It defines whether EFIFO, FIFOTHR, and PRETRK parameters of the Configure command can be reset to their default values by a software reset. See LOCK command.
MF FM or MFM. IF FM is 0, FM mode is selected. IF it is 1, MFM selected.
MT Multitrack. If MT is 1 after finishing Read/Write operation on side 0, FDC will automatically start searching for sector 1 0n side 1.
N N stands for the number of bytes written in a sector. if N is 00, then the sector size is 128 bytes. The number of bytes transferred is determined by DTL. Otherwise the sector size is (2 raised to the N'th power) times 128. All values up to 07(hex) are allowable.

N	Sector size
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
	- - -
07	16 bytes

NCN New Cylinder Number. It is going to be reached as a result of the seek operation. Desired position of head.

ND Non-DMA mode. When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the Host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode. interfacing to a DMA controller by means of the DRQ and DACK signals.

OW The bits denoted D0, D1, D2, and D3 of the perpendicular Mode command can only be overwritten when this bit is set to 1.

PCN Present Cylinder Number. The current position of the head at the completion of sense Interrupt Status command.

POLL Polling Disable. When set to 1, the internal polling routine is disabled. When 0, polling is enabled.

PRETRK Precompensation start track number. Programmable from track 00H to FFH.

R Sector address. The sector number toe read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.

RCN Relative Cylinder Number. Relative cylinder offset from present cylinder as used by the Relative Seek command.

SC Number of Sectors. The number of sectors to be initialized by the format command. The number of sectors to be verified during a Verify command, When EC is set to 1.

SK Skip. When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to 0, the sector is read or written the same as the Read and Write commands.

SRT Step Rate Time. The time interval between step pulse issued by the FDC. Programmable from 0.5 to 8ms, increments of 0.5ms at the 1 Mbps data rate. See Specify command.

ST0-3 Status register 0-3. It stands for one of the four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. ST0-3 may be read only after a command has been executed and contains information relevant to that particular commands.

STP During a scan operation, if STP is set to 1, the data in contiguous sectors is compared byte by byte with data sent from the Host; if STP is set to 2, then alternate sectors are read and compared.

COMMAND DESCRIPTION

During the command phase, the main status register must be polled by the host before each byte is written into the data register. The DIO(bit6) and RQM(bit7) bits in the main status register must be in the 0 and 1 states respectively. before each byte of the command may be written into the FDC. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to 1 and 0 states respectively.

Read Data

A set of nine byte words are required to placed the FDC into the Read Data mode. After the Read Data command has been issued, the FDC loads the head, if it is in the unloaded state, waits the specified head settling time defined in the specify command and begins regarding ID address mark and ID fields. When the current sector number stored in the ID register compares with the sector number read off the diskette, then the FDC outputs data from the data field byte by byte to the main system via FIFO.

After completion of the read operation from the current sector, the sector number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous function is called a multi sector read operation. The Read Data command must be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor. but will continue to read data from the current sector. check CRC Cycle Redundancy Count1 bytes, and then at the end of the sector terminate the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon MT(multitrack), MF(MFM/FM), and N(number of bytes/sector). Table 4-20 lists the transfer capacity.

Table 4-20. Transfer Capacity

Multitrack MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of sectors)	Final Sector Read from Diskette
0 0	0 1	00 01	(128) (26) = 3,328 (256) (26) = 6,656	26 at side 0 or 26 at side 1
1 1	0 1	00 01	(128) (52) = 6,656 (256) (52) = 13,312	 26 at side 1
0 0	0 1	01 02	(256) (15) = 3,840 (512) (15) = 7,680	15 at side 0 or 15 at side 1
1 1	0 1	01 02	(256) (30) = 7,680 (512) (30) = 15,360	 15 at side 1
0 0	0 1	02 03	(512) (8) = 4,096 (1024) (8) = 8,192	8 at side 0 or 8 at side 1
1 1	0 1	02 03	(512) (16) = 8,192 (1024) (16) = 16,384	 8 at side 1

The multitrack function (MT) allows the FDC to read data from both sides of the diskette. for a particular cylinder. Data will be transferred starting at sector 1, side 0 and completing at sector L, side 1 (sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette. When N = 0, then DTL defines the data length which the FDD must treat as a sector. If DTL is smaller than the actual data length in a sector, the data beyond DTL in the sector is not sent to the FIFO, The FDC reads (internally) the complete sector performing the CRC check, and depending upon the manner of command termination, may perform a multi sector read operation. When N is non zero, then DTL has no meaning and should be set to FF (Hex).
At the completion of the Read Data command, The head is not unloaded until after Head Unload time interval (specified in the specify command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another

If the FDC detects the index hole twice without finding the right sector, then the FDC sets the CM (Control Mark) flag in status Register 2 to a 1, and terminates the Read Data command, after reading all the data in the sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data filed are not checked when SK = 1. Table 4-21 shows Sk effect on Read Data command.

Table 4-21. SK Effect on Read Data Command

SK	Data Type	Sector Read	CM bit (in ST2)	Description of results
0	Normal	Y	0	Normal Termination
0	Deleted	Y	1	No Further Sectors Read
1	Normal	Y	0	Normal Termination
1	Deleted	N	1	Sector Skipped

If the processor terminates a Read or Write operation in the FDC, then the ID information in the result phase is dependent upon the state of the MT bit and EOF byte. Table 4-22 shows the values for C,H,R and N, When the processor terminates the command.

Table 4-22. C,H,R and N values

MT	HD	Final Sector Transfer to Host	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	C+1	NC	1	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	NC	R+1	NC
1	0	Less than EOT	NC	NC	R+1	NC
	0	Equal to EOT	NC	1	1	NC
	1	Less than EOT	NC	NC	R+1	NC
	1	Equal to EOT	C+1	0	1	NC

NC (No change) : The same value as the one at the beginning of command execution

Read Deleted data

This command is the same as the read data command except that when the FDC detects a data field (and SK = 0), It will read all the data in the sector and set the CM flag in status Register 2 to a 1, and then terminate the command, if SK = 1, then the FDC skips the sector with the delta address mark and reads the next sector. Table 4-23 shows SK effect on Read Deleted Data command.

Table 4-23. SK Effect on Read Deleted Data command

SK	Data Type	Sector Read	CM bit (in ST2)	Description of result
0	Normal	Y	1	No Further Sector Read
0	Deleted	Y	0	Normal Termination
1	Normal	N	1	Sector Skipped
1	Deleted	Y	0	Normal Termination

Write Data

A set of nine bytes is required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID fields. When all four bytes loaded during the command (C,H,R,N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte by byte via FIFO and outputs it to the FDD. After writing data into the current sector, the sector number stored in R is incremented by one, and the next data field is written into. The FDC continues this multisector Write operation until the issuance of a TC signal. If a TC is sent to the FDC it continues writing into the current sector to complete the data field. If the TC is received while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets the DE(data error) flag of Status Register 1 to a 1 and terminates the Write Data command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)
The Write data command operates in much the same manner as the Read Data command. The following items are the same, and one should refer to the Read Data command for details;

- Transfer capacity
- EN(End of Cylinder) flag
- ND(No Data)flag
- Head Unload Time interval
- ID information when the processor terminates command
- Definition of DTL when N=0 and when N≠0

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address Mark is written at the beginning of the data field instead of the normal Data Address Mark.

Read a Track

This command is similar to the Read Data command except that this is a continuous read operation where the entire data field from each of the sectors is read. Immediately after sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and sets the ND flag of Status Register 1 to a 1 if there is no comparison . Multitrack or skip operations are not allowed with this command. This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it senses the index hole for the second time, it sets the MA(Missing Address mark) flag in Status Register 1 to 1 and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

Read ID

The Read ID command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read if no proper ID Address Mark is found on the diskette before the index hole is encountered for second time, then the MA flag in Status Register 1 is set to a 1 and if no data is found then the ND(No Data) flag is also set in Status Register 1 to a 1. The command is then terminated with bits 7 and bit 6 in Status Register 0 set to 0 and 1 respectively . During this command there is no data transfer between FDC and the Host except during the result phase.

Format a Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps. Address Marks, ID fields and data fields, per the IBM System 34 or 3740 format(MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL and D which are specified by the Host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID Field for each sectors is supplied by the Host; that is, four data bytes per sector are needed by the FDC for C, H, R and N.
After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector is formatted This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a index hole for the second time and it terminates the command. Table 4-24. 4-25 shows the relationship between N, SC and GPL, for various sector sizes.

Table 4-24. Typical Values for Formatting

Mode	Sector Size	Sector Code	EOT	Sector Gap*	Format GAP3**
	decimal	hex	hex	hex	hex
125 Kbps FM	128	0	12	7	9
	128	0	10	10	19
	256	1	8	18	30
	512	2	4	46	87
	1024	3	22	C8	FF
	2048	4	1	C8	FF
250 Kbps MFM***	256	1	12	A	C
	256	1	10	20	32
	512	2	8	2A	50
	512	2	9	2A	50
	1024	3	4	80	F0
	2048	4	2	C8	FF
	4096	5	1	C8	FF
250 Kbps FM	128	0	1A	7	1B
	256	1	F	B	2A
	512	2	8	1B	3A
	1024	3	4	47	8A
	2048	4	2	C8	FF
	4096	5	1	C8	FF
500 Kbps MFM***	256	1	1A	E	36
	512	2	F	1B	54
	512	2	12	1B	6C
	1024	3	8	35	74
	2048	4	4	99	FF
	4096	5	2	C8	FF
	8192	6	1	C8	FF

* : Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections
** : Suggested values of GPL in format command
*** : In MFM mode. FDC cannot perform a Read/Write/Format operation with 128 bytes/sector (N=0)

Table 4-25. Typical Values for PC Compatible Diskette Media

Media Type	Sector Size	Sector Code	EOT	Sector Gap	Format Gap 3
	Decimal	hex	hex	hex	hex
360K	512	2	9	2A	50
1.2M	512	2	F	1B	54
720K	512	2	9	1B	50
1.44M	512	2	12	1B	6C
2.88M	512	2	24	1B	53

< System 34 Format Double Density >

GAP 4a 80x 4E	SYNC 12x 00	IAM		GAP 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 22x 4E	DATA AM		DATA	CRC	GAP3	GAP4b
		3x C2	FC			3x A1	FE							3x A1	FB FB				

< System 3740 Format Single Density >

GAP 4a 80x FF	SYNC 12x 00	IAM	GAP 25x 4E	SYNC 6x 00	IDAM	CYL	HD	SEC	NO	CRC	GAP2 11x 4E	SYNC 6x 00	DATA AM	DATA	CRC	GAP3	GAP4b
		FC			FE								FB or F8				

< Perpendicular Format >

GAP 4a 80x 4E	SYNC 6x 00	IAM		GAP 50x 4E	SYNC 12x 00	IDAM		CYL	HD	SEC	NO	CRC	GAP2 41x 4E	SYNC 12x 00	DATA AM		DATA	CRC	GAP3	GAP4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

Scan commands

The Scan commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compared the data on a byte by byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{HOST}$, $D_{FDD} \leq D_{HOST}$, $D_{FDD} \geq D_{HOST}$. The hexadecimal byte of FF either from memory of from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison [FF=largest number , 00=smallest number]. After a whole sector of data is compared , if the conditions for scan are met [equal , low or high], the last sector on the track is reached [EOT], or the terminal count signal is received. If the conditions for scan are met , then the FDC sets the SH(Scan Hit) flag of Status Register 2 to a 1 and terminates the Scan command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder[EOT], then the FDC sets the SN(Scan Not satisfied)flag of Status Register2 to a 1 and terminate the Scan command . The receipt of a TC signal from the Host or DMA controller during the scan operation will cause the FDC to comparison of the particular byte which in process and then to terminate the command . Table 4-26 shows the status of bits SH and SN under various conditions of Scan.

Table 4-26. Status of bits SH and SN

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0 1	1 0	Disk Data = Host Data Disk Data ≠ Host Data
Scan Low or Equal	0 0 1	0 0 0	Disk Data = Host Data Disk Data < Host Data Disk Data > Host Data
Scan High or Equal	0 0 1	1 0 0	Disk Data = Host Data Disk Data > Host Data Disk Data < Host Data

If the FDC encounters a Delete Data Address Mark on one of the sector (and SK=0) , then it regards the sector as the last sector on the cylinder , sets the CM(Control Mark) flag of Status Register 2 to a 1 and terminates the command . If SK = 1, the FDC skips the sector with the Deleted Address Mark and reads the next sector. In the second case (SK = 1) , the FDC sets the CM(Control Mark) flag of Status Register 2 to a 1 in order to show that a deleted sector had been encountered.

When either the STP (contiguous sectors = 01 , or alternate sector = 02) sectors are read or the MT(Multi Track) is programmed , it is necessary to remember that the last sector on the track must be read . For example , if STP = 02 , MT = 0 , the sector are numbered sequentially 1 through 26 and the Scan command is started at sector 21 , the following will happen : sector 21, 23 , aand 25 will be read , then the next sector(26) will be skipped and the index hole will encountered before the EOT value of 26 can be read . This will result in an abnormal termination of the command . If the EOT had been set st 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

Seek

The read / write head within the FDD is moved from cylinder to cylinder under the control of the Seek command . FDC has four independent Present Cylinder Registers each drive. they are cleared only after the Recalibrate command . The FDC compares the PCN(Present Cylinder Number) which is the current head position with the NCN(New Cylinder Number) , and if there is a difference , performs the following operation :

PCN < NCN : Direction signal to FDD set to a 1 , and step pulses are issued (In)

PCN > NCN : Direction signal to FDD set to a 0 , and step pulses are issued (Out)

The rate art which step pulses are issued is controlled by SRT(Stepping Rate Time) in the Specify command . After each step pulse is issues NCN is compares against PCN , and when NCN = PCN , the SE(Seek End) flag is set in Status Register 0 to a 1 , and the command is terminated . At this point FDC interrupt goes high . Bits0-3 in the Main Status Register are set during the Seek operation , and are cleared by the Sense Interrupt States command . During the command phase of the Seek operation , the FDC is in the FDC busy state . But during the execution phase , it is the non -busy state . While the FDC is in the non-busy state , another Seek command may be issued for as long as the FDC is in the process of sending step pulses to any drive.

If the time to write three bytes of Seek command exceeds 150μs, between the first two step pulses may be shorter then set in the Specify command by as much as 1ms

Recalibrate

The function of this command is to retract the read /write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD . As long as the Track 0 signal is low , the directionsignal remains 0 and step pulses are issued . When the Track 0 signal goes 1, the SE(Seek End) flag in States Register 0 is set to a 1 and the command is terminated. If the Track 0 signal is still 0 after 255 step pulses have been issued , the FDC sets the SE and EC(Equipment Check) flags of Status Register 0 to both 1s , and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

The ability to do overlap Recalibrate commands to multiple FDDs and load of the Ready signal , as described the Seek command , also applies to Recalibrate command.

Sense Interrupt Status

An Interrupt signal is generated by the FDC for one of the following reasons :

1. Upon entering the result phase of :
   a. Read Data command
   b. Read a Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format a Track command
   g. Write Deleted Data command
   h. Scan commands
   i. Verify command
2. Read line of FDD changes state
3. End of Seek or Recalibrate command
4. During execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and easily discernible by the processor . During an execution phase in non-DMA,bit4 in the Main Status Register is 1. Upon entering the result phase , this bit gets cleared . Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by read /write data to the FDC . Interrupts caused by reason 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status command . this command , when issued results the Interrupt signal and via bits 5,6,and 7 of Status Register 0 identifies the cause of the interrupt.

Table 4-27 . Status Register 0 Termination Codes

Seek End	Interrupt Code		Cause
Bit5	Bit6	Bit7	
0	1	1	Ready line changed state
1	0	0	Normal Seek or Recalibrate Termination
1	1	0	Abnormal Seek or Recalibrate Termination

The Sense Interrupt Status command is used in conjunction with the Seek or Recalibrate commands which have no result phase . When the disk drive has reached the desired head position , the FDC will set the Interrupt line true . The Host must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt , which could be Seek End of a change in ready status from one of the drives .

Specify

The Specify command sets the initial values for each of the three internal timers. the HUT(Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state . This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms , 02 = 32ms , ... ,0F = 240ms) . The SRT (Step Rale Time) defines the time interval between adjacent slop pulses . This timer is programmable from 1 to 16ms in increments of 1ms (F = 1ms , E = 2ms , D = 3ms ... 0 = 16ms) . The HLT(Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. This timer is programmable from 2 to 254ms in increments of 2ms (01 = 2ms , 02 = 4ms , 03 = 6ms ... 7F = 254ms) . The timeintervals mentioned above are affected by the data rate . The values are for 500Kbps MFM (250Kbps FM) . For a 300Kbps MFM data rate(150Kbps FM) , these values should be multiplied by 1.6667 and or 250 Kbps MFM (125Kbps FM) , these values should be doubled . For 1Mbps MFM , the values should be divides by 2. The choice of DMA or non-DMA operation is made by the ND (Non-DMA) bit. When this bit is high (ND = 1) the Non-DMA mode id deleted and when ND=0 , the DMA mode is selected.

Sense Drive Status

This command may be used by the Host whenever it wished to obtain the status of the FDDs . Status Register 3 contains the drive status information stored internally in FDC register.

Verify

This command is used to verify the data stored on disk , and acts exactly like a Read Data command except that no data is transferred to the host . Data is read from the disk . CRC compiled and checked against the previously stored value.
Because no data is transferred to the Host . TC cannot be used to terminate this command . By setting the EC bit to 1 , an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decrement to 0 (an SC value of 0 will verify 256 sectors) . This command can also be terminated by setting the EC bit to 0 and the EOT value equal to the final sector to be checked . If EC is set to 0 DLT/SC should be programmed to FFH . Refer to Table 4-22 and 4-28 for information concerning the values of MT and EC versus SC and EOT value.

Table 4-28. Verify Command Result Phase Table

MT	EC	SC/EOT Value	Termination Result
0	0	SC = DTL(FFH) EOT ≤ # Sectors per Side	Successful Termination Result Phase Valid
0	0	SC = DTL(FFH) EOT > # Sectors per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining and EOT ≤ # Sectors per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining or EOT > # Sectors per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL(FFH) EOT ≤ # Sectors per Side	Successful Termination Result Phase Valid
1	0	SC = DTL(FFH) EOT > # Sectors per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining and EOT ≤ # Sectors per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining or EOT > # Sectors per Side	Unsuccessful Termination Result Phase Invalid

1. # Sectors per Side : Number of formatted sectors per each side of the disk.
2. # Sectors Remaining : Number of formatted sectors left which can be read including side 1 of the disk if MT is set to 1.
3. If MT is set to 1 and SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Version

The Version command can be used to determine the FDC being used. The result phase uniquely identifies the FDC version. The FDC returns a value of 90H in order to be compatible with the 82077 of Intel. The NEC765 compatible FDC will return a value of 80H (invalid command).

Relative Seek

The command is coded the same as for Seek except for the MSB of the first byte and the DIR bit.

DIR : Head Step Direction Control

0 = Step Head Out

1 = Step Head In

RTN : Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

This command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time

The controller will issue RTN number of step pulses and update the Present Cylinder Number register (PCN) for the selected drive. The one exception to this is if the Track 0 signal goes active, which indicated that the drive read/write head is at the outermost track. In this case, the step pulses for the Relative Seek are terminated, and the PCN value is set according to the actual number of step pulses issued. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

After the step operation is complete, the controller will generate an interrupt. There is no result phase . No other command except the Sense Interrupt command should be issued while a Relative Seek command is in progress. A Relative Seek can be used instead of the normal Seek but the Host is required to calculate the difference between the current head location and the new (target) head location. This may require the Host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be.

Lock

This command allows the user full control of the FIFO parameters after a software reset. If the LOCK bit is set to 1, then the FIFO, THRESH, and PRETRK bits in the Configure command are not affected by a software reset. If the LOCK is 0 (default after a hardware reset), then the above bits will be set to their default values retain the other FIFO parameter values (such as THRESH) after a software reset.

After the command byte is written, the result byte must be read before continuing to the next command. The extraction of the Lock command is not performed until the result byte is read by the Host. If the part is reset after the command byte is written but before the result byte is read, then the Lock command execution will not be performed. This is done to prevent accidental execution of the Lock command.

Perpendicular Mode

This command is designed to support the unique Format and Write Data requirements of Perpendicular (Vertical) Recording disk drives(4Mbytes unformatted capacity). The Perpendicular Mode command will configure each of the four logical drives as a perpendicular of conventional disk drive. Configuration of the four logical disk drives is done via the D3-0 bits or with the CAP and WG control bits This command should be issued during the initialization of the floppy controller.

Perpendicular Recording drives operate in Extra High Density mode at 1Mbps and are downward compatible with 1.44 Mbyte and 720 Kbyte drives at 500 Kbps(High Density) and 250 Kbps(Double Density) respectively. If perpendicular drives are present in the system, this command should be issued during initialization of the FDC, which will configure each drive as perpendicular or conventional. Then when a drive is accessed for a Format or Write Data command, the FDC will adjust the Format or Write Data parameters based on the data rate.

Table 4-29. Effects of WGATE and GAP Bites on Format and Write commands

GAP	WG	Mode	GAP2 Length Written During Format	Portion of GAP2 Rewritten by Write Data Command
0	0	Conventional	22bytes	0 bytes
0	1	Perpendicular (≤500Kbps)	22bytes	19bytes
1	0	Reserved (Conventional)	22bytes	0 bytes
1	1	Perpendicular (1Mbps)	41bytes	38bytes

Looking at the second-command byte, DC3-0 correspond to the four logical drives. A 0 written to DCn sets drive n to conventional mode, and a 1 sets drive n to perpendicular mode. Also, the OW(Overwrite) bit offers additional control. When OW = 1, changing the values of DC3-0 (drive configuration bits) is enabled. When OW=0, the internal values of DC3-0 are unaffected, regardless of what is written to DC3-0.
The function of the DCn bits must also be qualified by setting both WG and GAP to 0. If WG and GAP are used i.e. not set to 00 they will override whatever is programmed in the DCn bits. Table 4-26 indicates the operation of the FDC based on the values of GAP and WG. Note that when GAP and WG are both 0, the DCn bits are used to configure each logical drive as conventional or perpendicular. DC3-0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset. A hardware reset will reset all the bits to zero (conventional mode for all drives). The Perpendicular Mode command bits may be rewritten at any time.

Perpendicular Recording type disk drives have a Pre-Erase Head Which leads The Read/Write Head by 200 μm, which translates to 38 bytes at the 1 Mbps data transfer rate(19 bytes at 500 Kbps). The increased spacing between the two heads requires a larger GAP2 between the Address Field and Data Field of a sector at 1Mbps. This GAP2 length of 41 bytes(at 1Mbps) will ensure that the Preamble in the Data Field is completely pre-erased by the Pre-Erase Head. Also, during Write Data operations to a perpendicular drive a portion of GAP2 must be rewritten by the controller to guarantee that the Data Field Preamble has been pre-erased..

Configure

This command will control some operation modes of the controller. It should be issued during the initialization of the FDC after power up. The function of the bits in the Configure registers are described below. These bits are set to their default values after a hardware reset. The value of each bit after a software reset is explained. A Configure command need not be issued if the default values of the FDC meet the system requirements

Configure Default Values:

EIS : No Implied Seeks
EFIFO : FIFO Disabled
POLL : Polling Enabled
FIFOTHR : FIFO Threshold Set to 1 Byte
PRETRK : Pre-Compensation Set to Track 0

EIS : Enable implied Seek. When set to 1 the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO : A 1 puts the FIFO into the NEC765 compatible mode where the FIFO is disabled. This means data transfers are asked for on a byte by byte basis. Defaults to 1, FIFO disabled. The threshold defaults to 1.

POLL : Disable polling of the drives. Defaults to 0 polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR : The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A 00H selects one byte, FH selects 16bytes.

PRETRK : Pre-compensation start track number. Programmable from track 0 to 255. Defaults to track 0.. A 00H selects track 0. FFH selects 255.

Dumpreg

This command is designed to support system run-time diagnostics and application software development and debug.

Invalid

If an Invalid command is sent to the FDC(a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status Register are both 1, indicating to the Host that the FDC is in the result phase and the contents of Status Register 0 must be read. When the Host reads Status Register 0, it will find an 80H indicating an Invalid command was received. A Sense Interrupt Status command must be sent after a Seek or Recalibrate interrupt: otherwise the FDC will consider the next command to be an invalid command. In some applications, the user may wish to use this command as a No-Op command to place the FDC in a standby or No Operation state.

4.3 Serial Ports

Serial ports are completely independent. They perform serial-to-parallel conversion or parallel-to-serial conversion between a peripheral device or a modem and CPU.

Serial Ports Registers

Internal registers are classified by three types: data, status, and control registers. The data registers are the Receiver Buffer Register and the Transmitter Holding Register. The status registers are the Line Status Register and the Modem Status Register. Also the control registers are Divisor Latch LSB and Divisor Latch MSB for baud rate selection.

The system programmer may be accessed any of the UART registers summarized in Table 4-19 via the CPU. These registers control UART operations including transmission and reception of data.

Receive Buffer Register (RBR)

This read only register holds the received incoming data byte.

Transmit Holding Register (TUR)

This write only register contains the data to be transmitted.

Line Control Register (LCR)

The system programmer specifies the format of the asynchronous data communication exchanges and sets the Divisor Latch Access bit via the Line Control Register (LCR). The programmer can also read the contents of the Line Control Register. The read capability simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. Table 4-30 shows the contents of the LCR. Details on each bit follow:

Bit 0 and 1 : These two bits specify the number of bits in each transmitted or received serial character.The encoding of bit 0 and 1 is as follows.

Table 4-30. The contents of the LCR.

Bit 1	Bit 0	Character Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2 : This bit specifies the number of stop bits transmitted and received in each serial character. If bit 2 is logic 0, one stop bit is generated in the transmitted data. If bit 2 is logic 1 when a 5-bit word length is selected via bit 0 and 1, one and a half stop bits are generated. If bit 2 is logic 1 when either a 6-,7-, or 8-b bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only regardless of the number of stop bit selected.

Bit 3 : This bit is the Parity Enable bit. When bit 3 is logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4 : This bit is the Even Parity Select bit. When bit 3 is logic 1 and bit 4 is logic 0, odd number of logic 1s is transmitted or checked in the data word bits and parity bit. When bit 3 is logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5 : This bit is the Stick Parity bit. When bit 3,4 and 5 are logic 1, the parity bit is transmitted and checked as logic 0. If bit 3 and 5 are 1 and bit 4 is logic 0, then the parity bit is transmitted and checked as logic 1. If bit 5 is logic 0, Stick parity is disabled.

Bit 6 : This bit is the Break Control bit. When it is set to logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

* Note : This feature enables the CPU to alert a terminal. During the break, the transmitter can be used as a character time to accurately establish the break duration in a computer communication system.

Bit 7 : This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a read or write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Line Status Register

This register provides status information to the CPU concerning the data transfer. Table 4-30. shows the contents of the Line Status Register. Details on each bit follow :

Bit 0 : This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1 : This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the which causes elimination of the previous character. The OE indicator is set to logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. The OE is indicated to the CPU as soon as it happens. The character in the shift register is overwritten, but it is not transferred to the FIFO.

Bit 2 : This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to logic 0 whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is detected by CPU when its associated character is at the top of the FIFO.

Bit 3 : This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character does not have a valid stop bit. Bit 3 is set to logic 1 whenever the stop bit following the last data bit or parity bit is detected as logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to. This error is detected by the CPU when its associated character is at the top of the FIFO. The UART will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit so it samples this 뱒tart?bit twice and then takes in the 뱸ata?

Bit 4 : This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time. (that is, the total time of start bit + data bits + parity + stop bit). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. In the FIFO mode, this error is associated with the particular character in the FIFO it applies to.

This error is detected by the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is enabled after SIN goes to the marking state and receives the next valid start bit.

Note : Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5 : This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmitter Holding Register Empty Interrupt enable is set high. The THRE bit is set to logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.In the FIFO mode, this bit is set when the XMIT FIFO is empty ; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6 : This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to logic 0 whenever either the THR or TSR has a data character. In the FIFO mode, this bit is set to one whenever both the transmitter FIFO and shift register are empty.

Bit 7 : In the GM16C450 Mode, this is logic 0. In the FIFO mode, LSR 7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR 7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

* Note : The Line Status Register is only for read operations. Writing to this register is not recommended as this operation is only used for factory testing.

FIFO Control Register

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signaling.

Bit 0 : Writing a 1 to FCR 0 enables both the XMIT and RCVR FIFOs. Resetting FCR 0 will clear all bytes in both FIFOs. When changing from FIFO Mode to GM16C450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1 : Writing a 1 to FCR 1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 written to this bit position is self-clearing.

Bit 2 : Writing a 1 to FCR 2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. This shift register is not cleared. The 1 written to this bit position is self-clearing.

Bit 3 : Setting FCR 3 to a 1 will cause the RXRDY and TXRDY pins to change from mode 0 to mode 1 if FCR 0 = 1

Bit 4,5 : FCR 4 and FCR 5 are reserved for future use.

Bit 6,7 : FCR 6 and FCR 7 are used to set the trigger level for the RCVR FIFO interrupt.

Table 4-31. RCVR FIFO

7	6	RCVR FIFO Trigger Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Interrupt Identification Register

In order to provide minimum software overhead during data character transfers, the UART identifies interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions are 1.Receiver Line Status ; 2.Received Data Ready ; 3.Transmitter Holding Register Empty ; and 4.in order of priority Modem Status. When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Details on each bit follow :

Bit 0 : This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is logic 1, no interrupt is pending.

Bit 1 and 2 : These two bits are used to identify the highest priority interrupt pending.

Bit 3 : In the GM16C450 Mode, this bit is 0. In the FIFO mode, this bit is set along with bit 2 when a timeout interrupt is pending.

Bit 4 and 5 : These two bits are always logic 0.

Bit 6 and 7 : These two bits are set when FCR 0 = 1

Table 4-32. Interrupt Identification Table

Bit 3	Bit 2	Bit 1	Bit 0	Priority	Type	Source	Reset Control
0	0	0	1	-	No interrupt	Receiver Line Status Error	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level
1	1	0	0	Second	Character Timeout Indication	During 4 character time the number of data in Receiver FIFO is not changed and there is at least 1 character in it	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR or Writing the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Modem Input Signal Change	Reading the Modem Status Register

Interrupt Enable Register

This register enables the five types of UART interrupts. Each interrupt can individually activate the interrupt (INT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to logic 1 enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the INT output signal. All other system functions operate in their normal manners, the Line Status and Modem Status Registers. Details on each bit follow.

Bit 0 : This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic 1.

Bit 1 : This bit enables the Transmitter Holding Register Empty Interrupt.

Bit 2 : This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3 : This bit enables the Modem Status Interrupt when set to logic 1.

Bit 4 through 7 : These four bits are always logic 0.

Modem Control Register

This register controls the interface with the Modem or data set (or peripheral device emulating a Modem). The contents of the Modem Control Register are indicated in Table 4-30 and are described below.

Bit 0 : This bit controls the Data Terminal Ready($\overline{DTR}$) output. When bit 0 is set to logic 1, the $\overline{DTR}$ output is forced to logic 0. When bit 0 is reset to logic 0, the DTR output is forced to logic 1.

* Note : The $\overline{DTR}$ output of the UART may be applied to an EIA inverting line driver (such as the GD75188) to obtain the proper polarity input at the succeeding Modem or data set.

Bit 1 : This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in an identical manner described above for bit 0.

Bit 2 : This bit controls the output 1($\overline{OUT1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the OUT1 output in an identical manner described above for bit 0.

Bit 3 : This bit controls the output 2($\overline{OUT2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the OUT2 output in an identical manner described above for bit 0.

Bit 4 : This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs; the transmitter Serial Output (SOUT) is set to the Marking (logic 1) State; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is looped back into the Receiver Shift Register input; the four Modem Control inputs (CTS, DSR, RI, and DCD) are disconnected; the four Modem Control outputs (DTR, RTS, OUT1, and OUT2) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, transmitted data is immediately received. This feature allows the processor to verify the transmit- and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The Modem Control Interrupts are also operational, but the interrupts sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bit 5 through 7 : These bits are always set to logic 0.

Modem Status Register

This register provides the current state of the control lines from the Modem (or Peripheral device) to the CPU. In addition to this current-state information, four bits of the Modem Status Register provide information change. These bits are set to logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem Status Register.

The contents of the MODEM Status Register are indicated in Table 4-30 and described next page.

Bit 0 : This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the CTS input to the chip has changed state since the last time it was read by the CPU.

Bit 1 : This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU

Bit 2 : This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3 : This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

* Note : Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated.

Bit 4 : This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to 1, this bit is equivalent to RTS in the MCR.

Bit 5 : This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to 1, this bit is equivalent to DTR in the MCR.

Bit 6 : This bit is the complement of the Ring Indicator (RI) input. If bit 4 of the MCR is set to 1, this bit is equivalent to OUT1 in the MCR.

Bit 7 : This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to 1, this bit is equivalent to OUT2 in the MCR.

Scratch Register

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR 0 = 1, IER 0 = 1) RCVR interrupts occur as follows :

1) The received data available interrupt will be issued to the CPU when the FIFO has reached its programmed trigger level; it will be cleared as soon as the FIFO drops below its programmed trigger level.

2) The IIR receive data available indication also occurs when the FIFO trigger level is reached, and like the interrupt, it is cleared when the FIFO drops below the trigger level.

3) The receiver line status interrupt (IIR-06), as before, has higher priority than the received data available (IIR-04) interrupt.

4) The data ready bit (LSR 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occurs as follows :

1) A FIFO timeout interrupt occurs if the following conditions exist :

- at least one character is in the FIFO

- the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed, the second one is included in this time delay).

- the most recent CPU read of the FIFO was longer than 4 continuous character times ago.

This will cause a maximum character received to interrupt issued delay of 160 ms at 300 baud with a 12 bit character.

2) Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).

3) When a timeout interrupt has occurred, it is cleared and the timer is reset when the CPU reads one character from the RCVR FIFO.

4) When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR 0 = 1, IER 1 = 1), XMIT interrupts occurs as follows :

1) The transmitter holding register interrupt (02) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

2) The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE = 1 and there has not been at least two bytes at the same time in the transmit FIFO since the last THRE = 1. The first transmitter interrupt affect changing FCR 0 will be immediate if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Operation

When FCR 0 = 1 resetting, IER 0, IER 1, IER 2, IER3 or all to zero puts the UART in the FIFO Polled Mode. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode.

Programmable Baud Generator

The UART contains a programmable Baud Generator. The output frequency of the Baud Rate Generator is 16× the Baud [divisor # = (frequency input) ÷ (baud rate × 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be located during initialization to ensure proper operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded.

Table 4-20. shows decimal divisors for baud rates. For baud rates of 38,400 and below, the minimal error is obtained. Using a divisor of zero is not recommended.

Table 4-33. Divisors, Baud Rates and Clock Frequencies

Divisor Baud Rate	(24 ÷ 13) MHz clock	
	Decimal Divisor for 16× Clock	Percent Error
50	2304	0.001
75	1536	
110	1047	
134.5	857	0.004
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.005
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	0.030
115200	1	0.16
230400	32770	0.16
460800	32769	0.16

InfraRed Interface

The GM82C803C has faculty of infrared interface. The IR interface provides a two-way wireless communication port using infrared. In GM82C803C, two ways of IR implementation (Amplitude Shift Keyed IR, IrDA) are provided.

IrDA supports up to 115K Baud rate in serial communication. Each word is sent serially beginning with a zero value start bit. ??is signaled by sending a single IR pulse, while ??is signaled by sending no IR pulse during the bit time.

The Amplitude Shift Keyed IR has baud rate up to 19.2Kbps. Each word is sent serially beginning with a zero value start bit. ??is signaled by sending a 500KHz pulse during the serial bit time, while ??is signaled by sending no transmission during the bit time.

If the Half Duplex option is chosen, there is a time interval while the direction of the transmission is changed. The interval timer starts after the last bit is transferred during a transmission and blocks the receiver input until the interval elapses. If a datum is loaded in transmitter fifo before the interval elapses, the timer is cleared. If a datum is loaded into the transmit buffer while a character is received, the transmission will not start for the interval after the last receive bit is received. If the start bit of another character is received during this time interval, the timer is cleared. The time-interval is four character times. One character time is defined as a 10 bit time regardless of the actual word length.

Table 4-34. Summary of Registers

	Register Address											
	0 DLAB=0	0 DLAB=0	1 DLAB=0	1	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	Modem Control Register	Line Status Register	Modem Status Register	Scratch Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt	??if Interrupt Pending	FIFO Enable	Word Length Select Bit 0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt	Interrupt ID Bit (0)	RCVR FIFO Reset	Word Length Select Bit 1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt	Interrupt ID Bit (1)	XMIT FIFO Reset	Number of Stop Bits	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt	Interrupt ID Bit (2) (Note 2)	DMA Mode Select	Parity Enable	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Trans-mitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	FIFO3 Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Trans-mitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	FIFO3 Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

5. Electrical Information

5.1 Absolute Maximum Rating

Symbol	Parameter	Rating	Units
Vdd	Supply Voltage	-0.5 ~ 7	V
Top	Operating Temperature	0 ~ 70	℃
Tstg	Storage Temperature	-65 ~ +165	℃
Vss	All input and Output Voltage with respect to Vss	-0.5 ~ Vcc+0.5	V
Pd	Power Dissipation	500	mW

5.2 DC Electrical Characteristics

(Vdd = 5V ± 5% Vss = 0V)

Symbol	Parameter	Condition	User Spec.		Units
			Min	Max	
V_{IH}	High Level Input Voltage		2.2	Vdd	V
V_{IL}	Low Level Input Voltage		-0.5	0.8	V
I_{CC}	Average Vdd Supply Current	Vdd= 5.25V , No loads on the Outputs		50	mA
I_{IH}	Input High Current	V_{IN} = 2.2V to Vdd		10	uA
I_{IL}	Input Low Current	V_{IN} = Vss to 0.8V	-10		uA

* Input hysterisis pins:

RESET, INDEX, TRK00, WRTPRT, RDATA, DSKCHG

5.2.1 Output Pins

4mA Buffer

(TXD1, TXD2/IRTX, $\overline{\text{RTS}}$, $\overline{\text{DTR}}$, $\overline{\text{IDEEN}}$, $\overline{\text{GAMECS}}$ **)**

Symbol	Parameter	Condition	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -1mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 4mA		0.4	V

8mA Buffer

(IRQ_A, IRQ_C, IRQ_D, IRQ_E, IRQ_F, DRQ_A, DRQ_B, DRQ_C, D0-D7)

Symbol	Parameter	Condition	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -8mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8mA		0.4	V

20mA Buffer

($\overline{\text{SLCTIN}}$, $\overline{\text{INIT}}$, $\overline{\text{AUTOFD}}$, $\overline{\text{STROBE}}$, PD7-PD0, IOCHRDY, IRQ_H, $\overline{\text{HDCS0/1}}$, IRQ_B)

Symbol	Parameter	Condition	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -12mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 20mA		0.5	V

40mA Buffer

($\overline{\text{DRVDEN}}$, $\overline{\text{MTR}}$, $\overline{\text{DS}}$, $\overline{\text{DIR}}$, $\overline{\text{STEP}}$, $\overline{\text{WDATA}}$, $\overline{\text{WGATE}}$, $\overline{\text{HDSEL}}$, $\overline{\text{ADRX}}$)

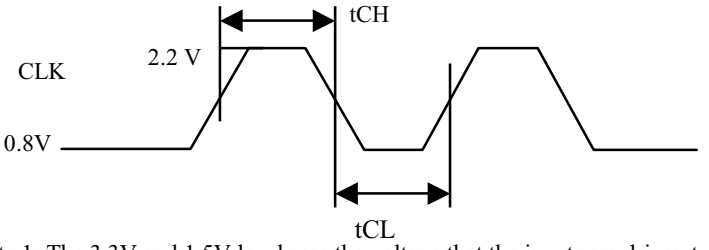
Symbol	Parameter	Condition	Min	Max	Units
VOL	Output Low Voltage	IOL = 40mA		0.4	V

5-3. AC Electrical Characteristics (Ta = 0 ℃ to + 70℃, Vdd = +5V ± 5%)

Symbol	Parameter	Condition	Min	Max	Units
CPU INTERFACE					
tAR	Delay from Address to $\overline{IOR}$		19		ns
tAW	Delay from Address to $\overline{IOW}$		19		ns
tCH	Duration of Clock High Pulse	External Clock (5M)	90		ns
tCL	Duration of Clock Low Pulse	External Clock (5M)	90		ns
tDH	Data Hold Time		10		ns
tDS	Data Setup Time		19		ns
tHZ	$\overline{IOR}$ to Floating Data Delay	(Note1)	13	25	ns
tMR	Master Reset Pulse Width		100		ns
tRA	Address Hold Time from $\overline{IOR}$		0		ns
tRC	Read Cycle Update		36		ns
tRD	$\overline{IOR}$ Strobe Width		60		ns
tRVD	Delay from $\overline{IOR}$ to Data			40	ns
tWA	Address Hold Time from $\overline{IOW}$		0		ns
tWC	Write Cycle Update		36		ns
tWR	WR Strobe Width		60		ns
RC	Read Cycle = tAR+tRD+tRC		115		ns
WC	Write Cycle = tAW+tWR+tWC		115		ns

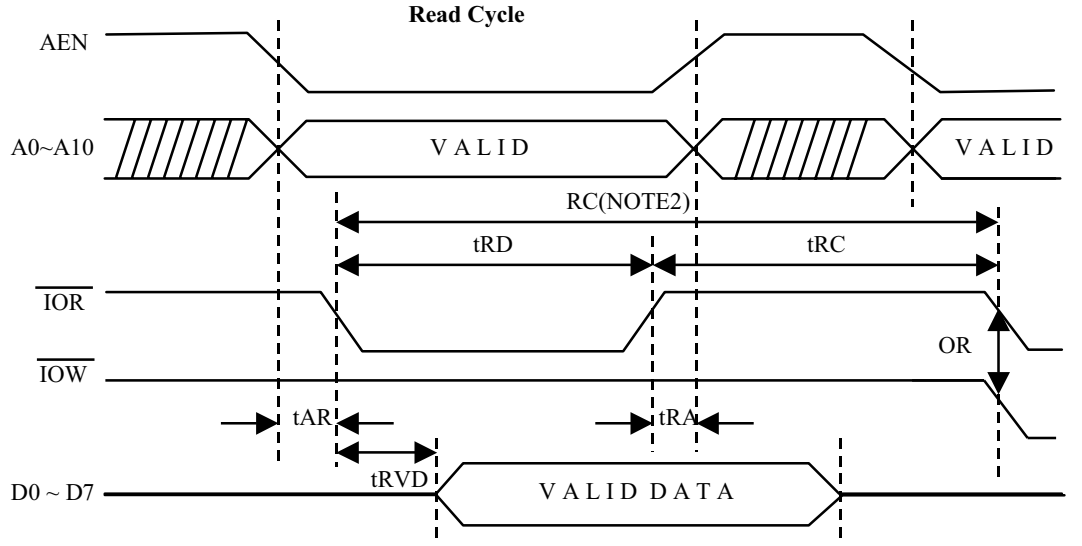
Note 1: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.
Note2 : All AC timings can be met with current loads that don't exceed 3.2 mA or -80uA at 100pF capacitive loading.
Note3 : For capacitive loads that exceed 100 pF, the following typical derating factors should be used:
100 pF < Cl ≤ 150 pF, t=(0.1ns/pF) (Cl-100 pF) typical
150 pF < Cl ≤ 200 pF, t=(0.08ns/pF) (Cl-100 pF) and
t = (0.5ns/mA) (Isink mA) or
t = -(0.5ns/mA) (Isource mA)
Isource is always negative, Isink ≤ 4.8mA, Isource ≤ -120uA, Cl ≤ 250 pF

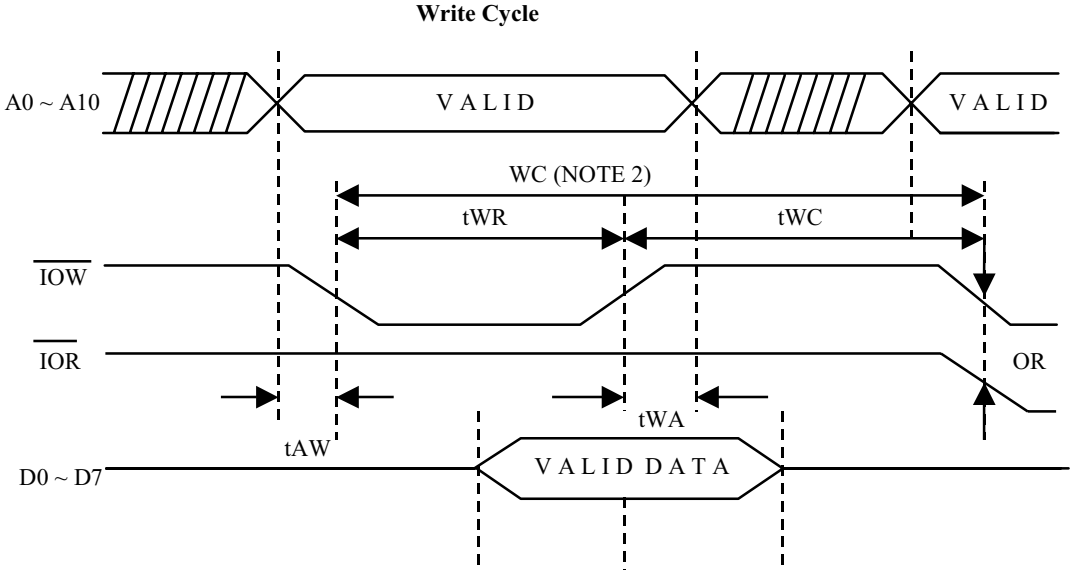
5-3.1 External Clock Input (14.318MHz)



* Note 1: The 3.3V and 1.5V levels are the voltage that the inputs are driven to during AC testing.

5-3.2 CPU Interface

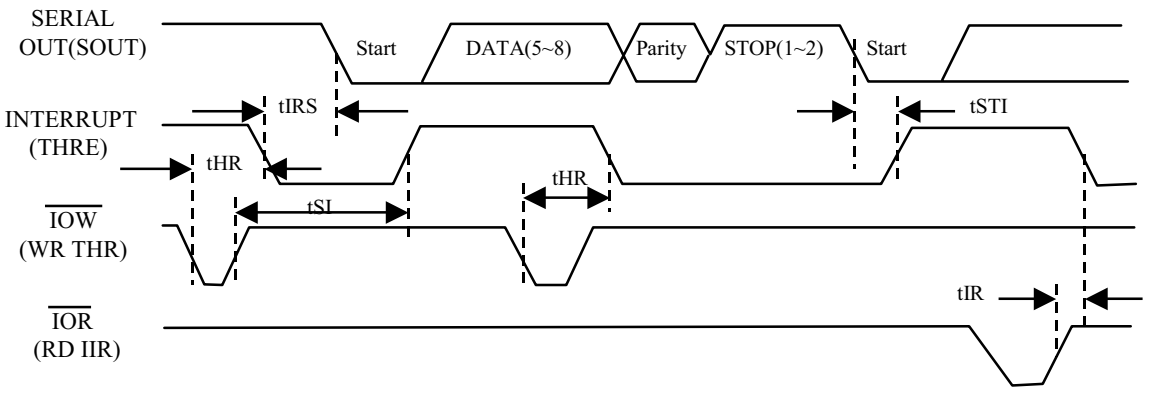




5-3.3 Transmitter

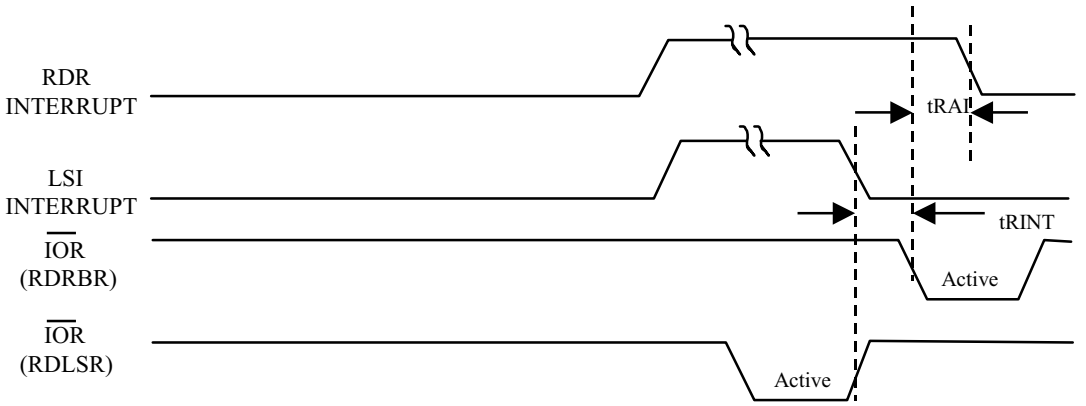
System	Parameter	User Spec		Units
		Min	Max	
tHR	Delay from $\overline{\text{IOW}}$(WR THR) to Reset Interrupt		175	ns
tIR	Delay from $\overline{\text{IOR}}$ (RD IIR) to Reset Interrupt (THRE)		250	ns
tIRS	Delay from Initial INTR Reset to Transmit Start	8	24	BAUDOUT Cycles
tSI	Delay from Initial Write to Interrupt	16	32	BAUDOUT Cycles
tSTI	Delay from Start to Interrupt (THRE)		8	BAUDOUT Cycles
tSXA	Delay from Start to TXRDY active		8	BAUDOUT Cycles
tWXI	Delay from Write to TXRDY inactive		195	ns

Transmitter Timing



5-3.4 Receiver

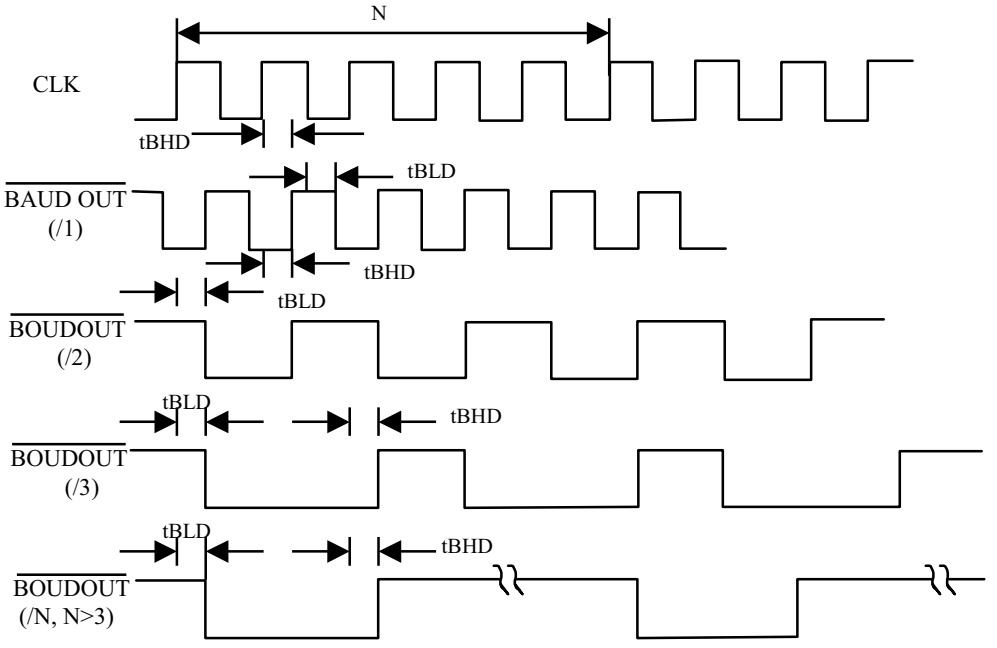
Symbol	Parameter	User Spec		Units
		Min	Max	
tRAI	Delay from Active Edge of $\overline{IOR}$ to Reset Interrupt		1	us
tRINT	Delay from Inactive Edge of $\overline{IOR}$ (RD LSR) to Reset Interrupt		1	us



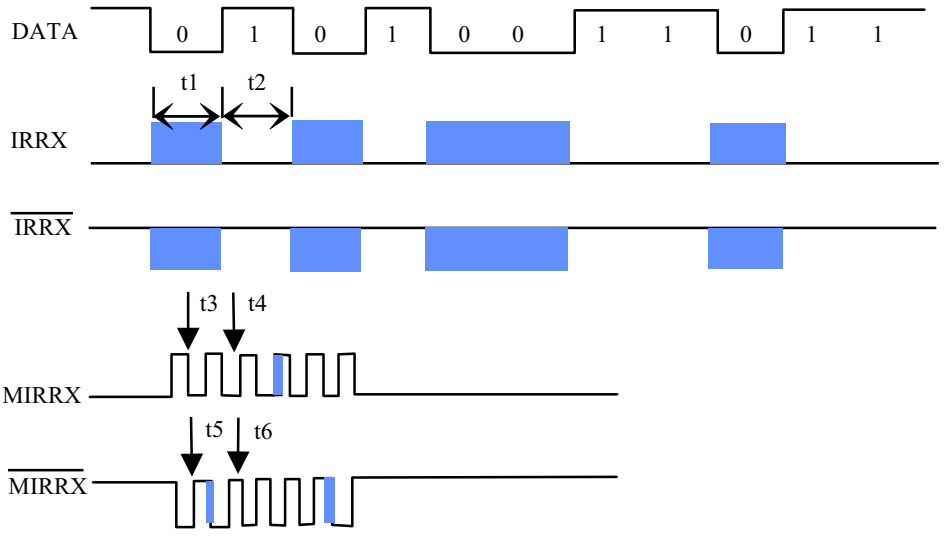
5-3.5 Serial Interface Baud Generator

Symbol	Parameter	User Spec		Units
		Min	Max	
N	Baud Divisor	1		
tBHD	Baud Output Positive Edge Delay		56	ns
tBLD	Baud Output Negative Edge Delay		56	ns

Baudout Timing



5-3.6 ASKIR



	Parameter	Min	Typ	Max	Units
t1	Modulated Output Bit Time				us
t2	Off Bit Time				us
t3	Modulated Output "On"	0.8	1	1.2	us
t4	Modulated Output "Off"	0.8	1	1.2	us
t5	Modulated Output "On"	0.8	1	1.2	us
t6	Modulated Output "On"	0.8	1	1.2	us

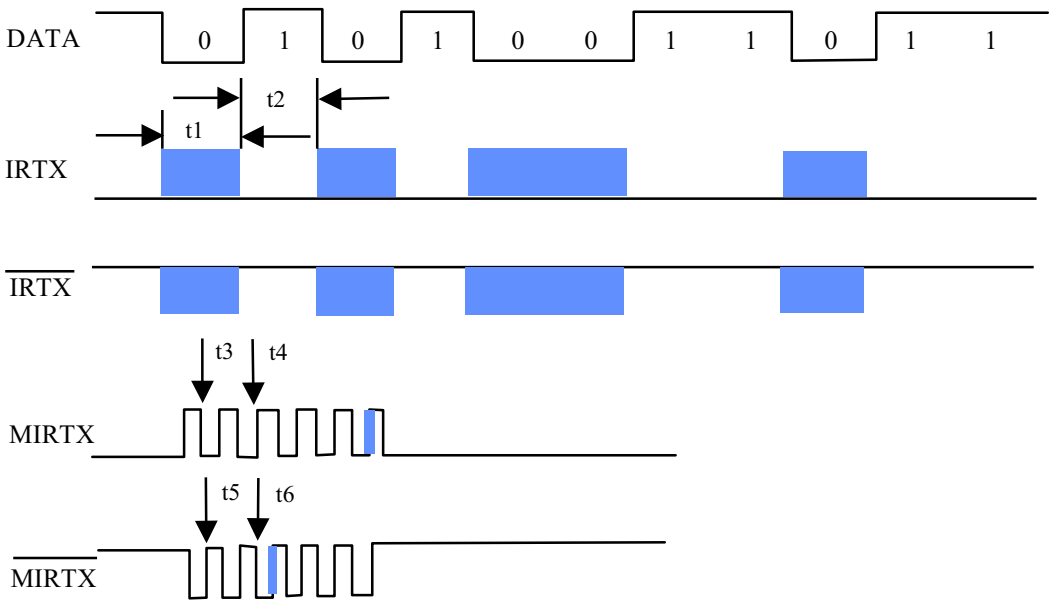
Notes :

1. IRRX : CRC Bit 0 : 1= RCV active iow

   $\overline{\text{IRRX}}$: CRC Bit 0 : 0 = RCV active high (default)

   MIRRX, $\overline{\text{MIRRX}}$ are the modulated outputs

FIGURE 1 - AMPLITUDE SHIFT KEYED IR RECEIVE TIMING



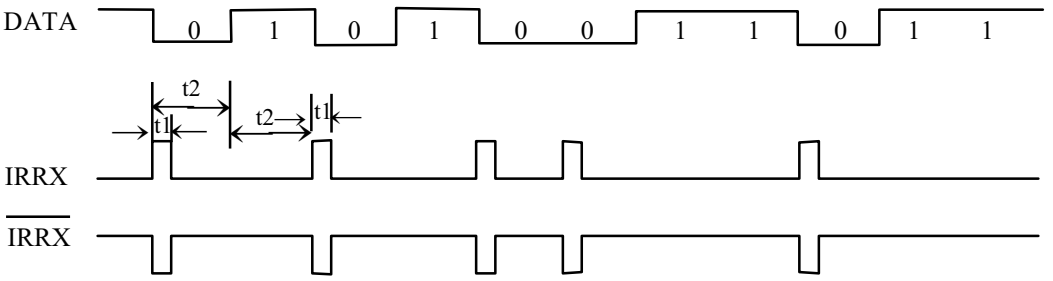
	Parameter	Min	Typ	Max	Units
t1	Modulated Output Bit Time				us
t2	Off Bit Time				us
t3	Modulated Output "On"	0.8	1	1.2	us
t4	Modulated Output "Off"	0.8	1	1.2	us
t5	Modulated Output "On"	0.8	1	1.2	us
t6	Modulated Output "On"	0.8	1	1.2	us

Notes :

1. $\overline{\text{IRTX}}$: CRC Bit 1 : 1= XMIT active iow
   $\overline{\text{IRTX}}$: CRC Bit 1 : 0 = XMIT active high (default)
   MIRTX, $\overline{\text{MIRTX}}$ are the modulated outputs

FIGURE2 - AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING

5-3.7 IrDA

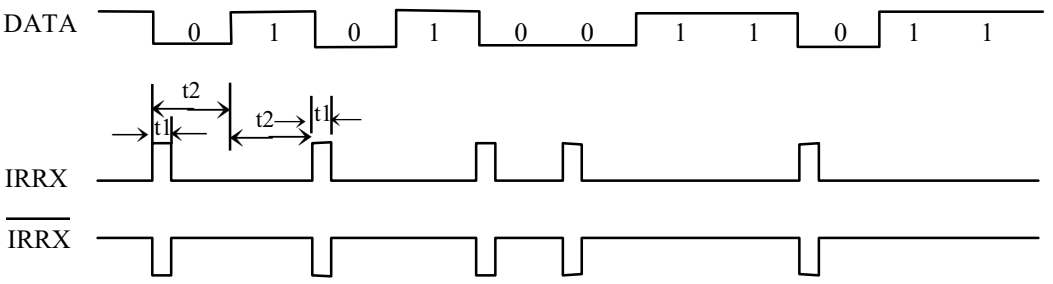


	Parameter	Min	Typ	Max	Units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	μs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	μs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	μs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	μs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	μs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	μs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	μs
t2	Bit Time at 115kbaud		8.68		μs
t2	Bit Time at 57.6kbaud		17.4		μs
t2	Bit Time at 38.4kbaud		26		μs
t2	Bit Time at 19.2kbaud		52		μs
t2	Bit Time at 9.6kbaud		104		μs
t2	Bit Time at 4.8kbaud		208		μs
t2	Bit Time at 2.4kbaud		416		μs

Notes :

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. TIR : CRC Bit 1 : 1 = XMIT active low
   $\overline{\text{TIR}}$: CRC Bit 1 : 0 = XMIT active high (default)

FIGURE3 - IrDA RECEIVE TIMING



	Parameter	Min	Typ	Max	Units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	μs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	μs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	μs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	μs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	μs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	μs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	μs
t2	Bit Time at 115kbaud		8.68		μs
t2	Bit Time at 57.6kbaud		17.4		μs
t2	Bit Time at 38.4kbaud		26		μs
t2	Bit Time at 19.2kbaud		52		μs
t2	Bit Time at 9.6kbaud		104		μs
t2	Bit Time at 4.8kbaud		208		μs
t2	Bit Time at 2.4kbaud		416		μs

Notes :

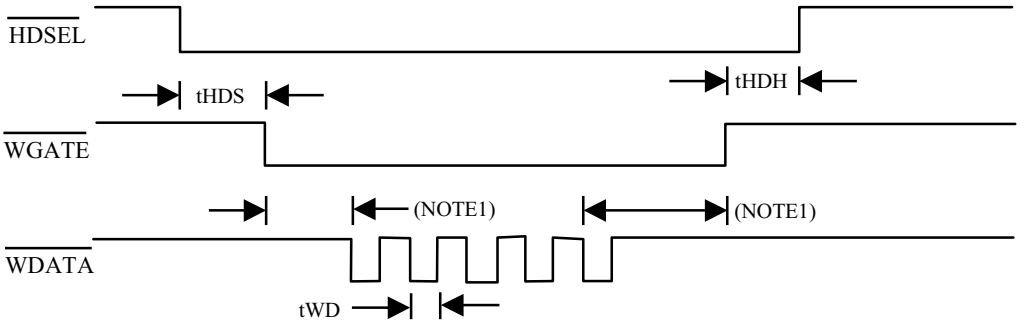
1. Receive Pulse Detection Criteria : A received pulse is considered detected if the received pulse is a minimum of 1.41us .
2. RIR : CRC Bit 0 : 1 = RCV active low
   $\overline{\text{RIR}}$: CRC Bit 0 : 0 = RCV active high (default)

FIGURE4 - IrDA TRANSMIT TIMING

5-3.8 Drive Write Timing

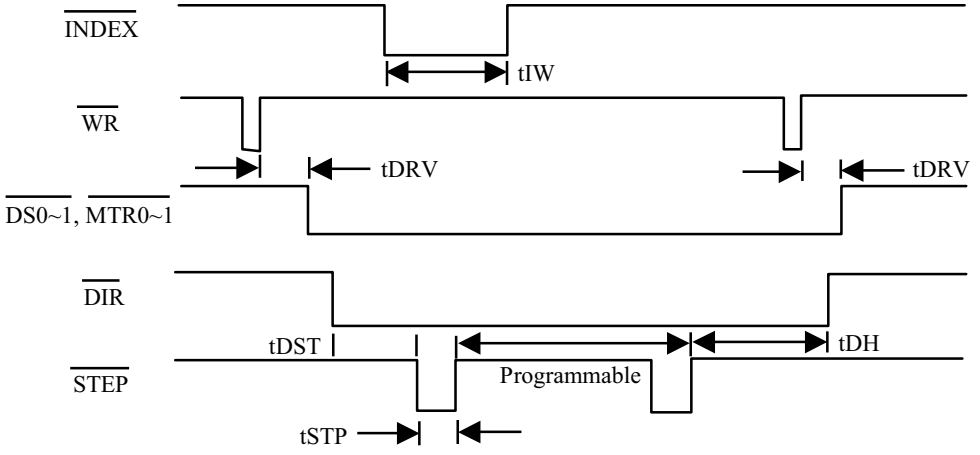
Symbol	Parameter	Condition	Min	Max	Units
tWD	Write Data Pulse Width	250 kb/s (MFM)	500		ns
tHDS	Head Select Setup to Write Assertion		40		us
tHDH	Head Select Hold from $\overline{\text{WGATE}}$		12		us
		300 kb/s (MFM)	416		ns
		500 kb/s (MFM)	250		ns
		1000 kb/s (MFM)	125		ns

Note 1 : Whenever $\overline{\text{WGATE}}$ is asserted the WDATA line is active. At the end of each write one dummy byte is written before $\overline{\text{WGATE}}$ is deasserted.



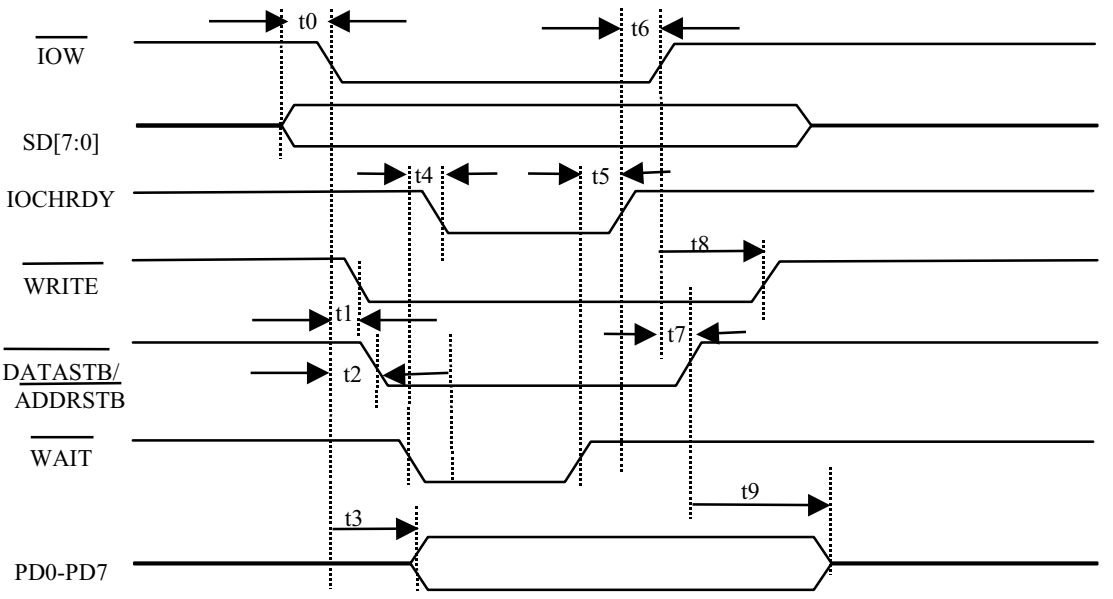
5-3.9 Drive Track Access Timing

Symbol	Parameter	Min	Max	Units
tDH	Direction Hold from End of Step	1 Step Time		
tDRV	Drive Select or Motor Time from Write Strobe		100	ns
tDST	Direction Setup prior to Step	6		us
tIW	Index Pulse Width	100		ns
tSTP	Step Pulse Width	6		us

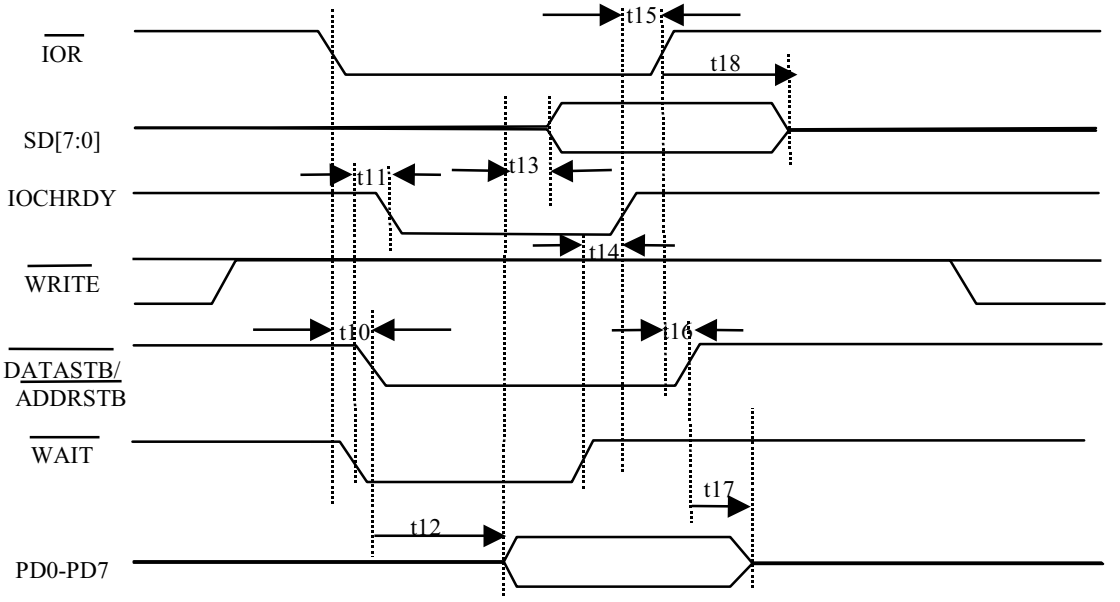


5-3.10 EPP

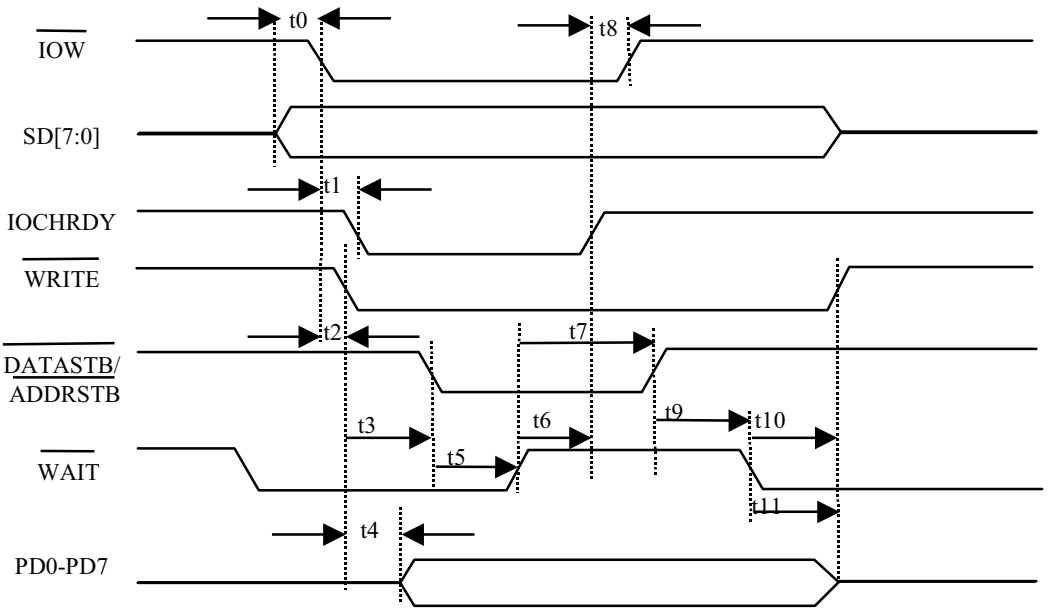
EPP 1.7 Write Timing



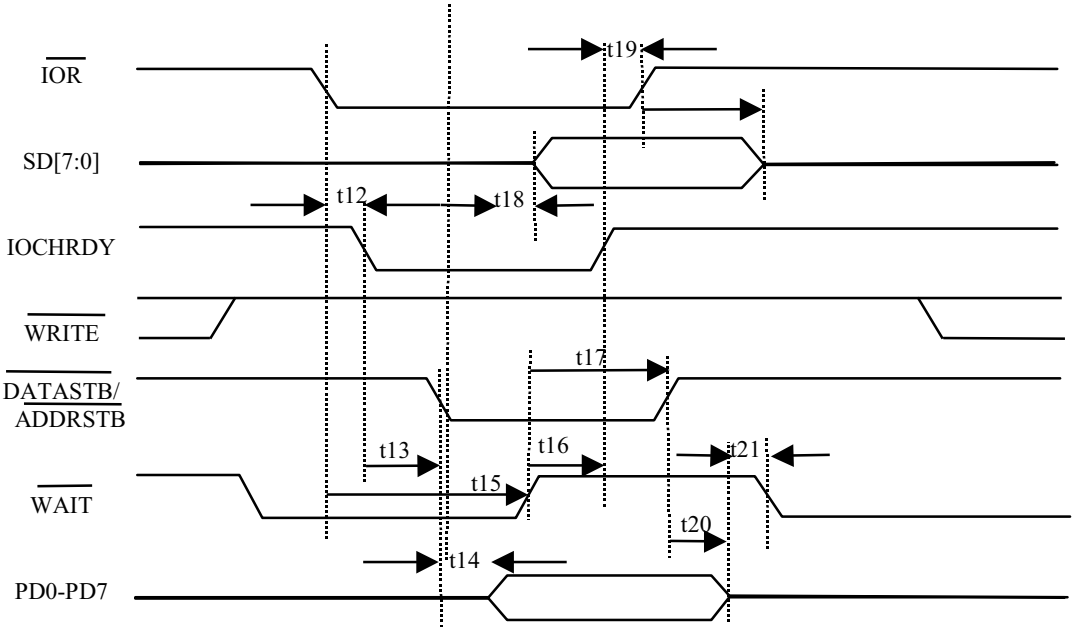
EPP 1.7 Read Timing



EPP 1.9 Write Timing



EPP 1.9 Read Timing



EPP 1.9 WRITE / READ Cycle Timing Parameters

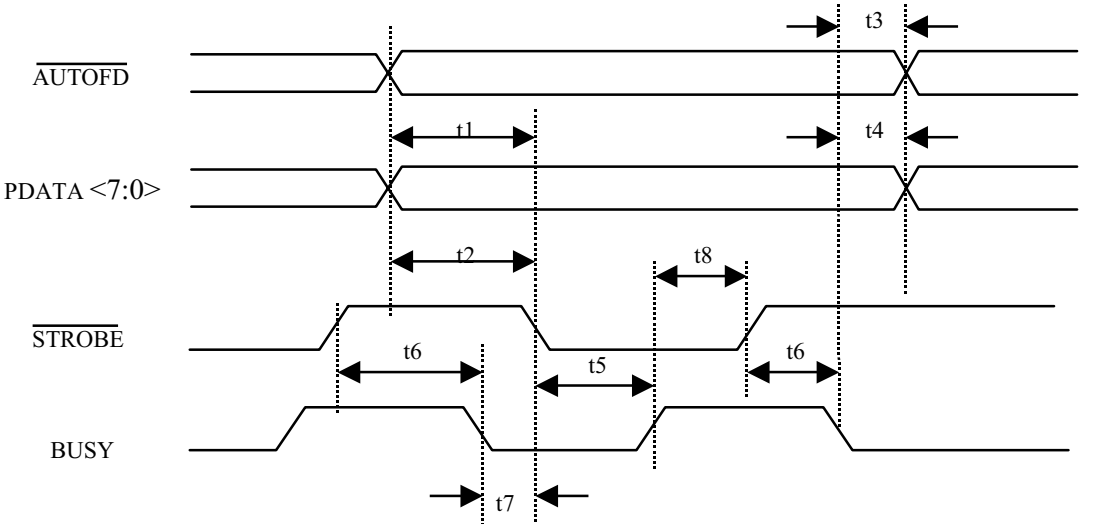
	Parameter	Min	Max	Unit	Note
t0	SD valid to IOW Asserted	0		ns	
t1	IOW Asserted to IOCHRDY Asserted	10	30	ns	
t2	IOW Asserted to WRITE Asserted		40		
t3	WRITE Asserted to command Asserted	40	80		
t4	WRITE Asserted to valid pdata	0			
t5	Command Asserted to WAIT Deasserted	0	10	us	
t6	WAIT Deasserted to IOCHRDY Deasserted	40	80		
t7	WAIT Deasserted to command Deasserted	120	160		
t8	IOCHRDY Deasserted to IOW Deasserted	10			
t9	Command Deasserted to WAIT Asserted	0			
t10	WAIT Asserted to WRITE Change	40	80		
t11	WAIT Asserted to invalid pdata	0			
t12	IOR Asserted to IOCHRDY Asserted	10	30		
t13	IOCHRDY Asserted to command Asserted	60	80		
t14	Command Asserted to valid pdata	0			
t15	Time out	0	10	us	
t16	WAIT Deasserted to IOCHRDY Deasserted	40	80		
t17	WAIT Deasserted to command Deasserted	120	160		
t18	Valid pdata to valid sdata	0	40		
t19	IOCHRDY Deasserted to IOR Deasserted	10			
t20	Command Deasserted to invalid pdata	0			
t21	Invalid pdata to WAIT Asserted	0			

EPP 1.7 WRITE / READ Cycle Timing Parameters

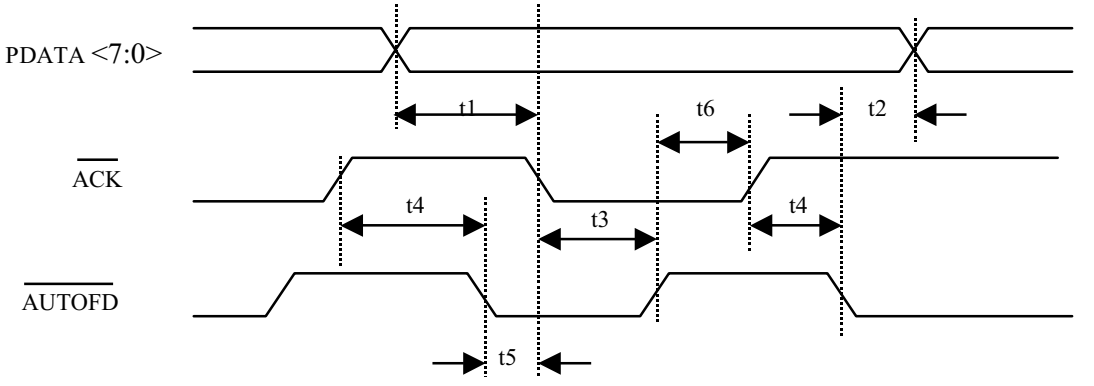
	Parameter	Min	Max	Unit	Note
t0	Valid sdata to IOW Asserted	0			
t1	IOW Asserted to WRITE Asserted	10	20		
t2	IOW Asserted to command Asserted	40	50		
t3	IOW Asserted to pdata valid	10	30		
t4	WAIT Asserted to IOCHRDY Asserted	10	20		
t5	WAIT Desserted to IOCHRDY Deasserted	10	20		
t6	IOCHRDY Deasserted to IOW Deasserted	10	20		
t7	IOW Deasserted to command Deasserted	40	60		
t8	IOW Deasserted to WRITE Deasserted	10	30		
t9	Command Deasserted to invalid pdata	0			
t10	IOR Asserted to command Asserted	40	60		
t11	WAIT Asserted to IOCHRDY Asserted	10	20		
t12	Command Asserted to pdata valid	0			
t13	Pdata valid to sdata valid	0	40		
t14	WAIT Deasserted to IOCHRDY Deasserted	10	20		
t15	IOCHRDY Deasserted to IOR Deasserted	10	30		
t16	IOR Deasserted to command Deasserted	40	60		
t17	Command Deasserted to pdata invalid	0			
t18	Sdata hold time	0	20		

5-3.11 ECP Interface

ECP Parallel Port Forward Timing



ECP Parallel Port Reverse Timing



	Parameter	Min	Max	Unit	Note
t1	$\overline{\text{AUTOFD}}$ Valid to $\overline{\text{STROBE}}$ Asserted	0	60	ns	
t2	PDATA Valid to $\overline{\text{STROBE}}$ Asserted	0	60	ns	
t3	BUSY Deasserted to $\overline{\text{AUTOFD}}$ Changed	80	180	ns	1, 2
t4	BUSY Deasserted to PDATA Changed	80	180	ns	1, 2
t5	$\overline{\text{STROBE}}$ Asserted to BUSY Asserted	0		ns	
t6	$\overline{\text{STROBE}}$ Deasserted to BUSY	0		ns	
t7	Deasserted	80	200	ns	1, 2
t8	BUSY Deasserted to $\overline{\text{STROBE}}$ Asserted BUSY Asserted to $\overline{\text{STROBE}}$ Deasserted	80	180	ns	2

1. Maximum value only applied if there is data in the FIFO waiting to be written out.
2. BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

ECP PARALLEL PORT FORWARD TIMING

	Parameter	Min	Max	Unit	Note
t1	PDATA Valid to $\overline{\text{ACK}}$ Asserted	0		ns	
t2	$\overline{\text{AUTOFD}}$ Deasserted to PDATA Changed	0		ns	
t3	$\overline{\text{ACK}}$ Asserted to $\overline{\text{AUTOFD}}$ Deasserted	80	200	ns	1, 2
t4	$\overline{\text{ACK}}$ Deasserted to AUTOFD Asserted	80	200	ns	2
t5	$\overline{\text{AUTOFD}}$ Asserted to $\overline{\text{ACK}}$ Asserted	0		ns	
t6	$\overline{\text{AUTOFD}}$ Dasserted to $\overline{\text{ACK}}$ Deasserted	0		ns	

1. Maximum value only applies if there is room in the FIFO and a terminal count has not been received. ECP can stall by keeping $\overline{\text{AUTOFD}}$ low.
2. $\overline{\text{ACK}}$ is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

ECP PARALLEL PORT RECEIVE TIMING