IT8705F APPLICATION CIRCUIT

SH1:IT8705F
SH2:FDC,LPT & COM,IR & CIR
SH3:FLASH ROM & VID CONTROL
SH4:GAME ,MIDI & SMART CARD READER
SH5:THERMISTOR & VOLTAGE MONITOR & FAN CONTROL
SH6:LAYOUT/ROUTING GUIDELINES

REVISION HISTORY

SCHEMATICS REVISION	PCB REVISION	DATE	MODIFICATION ITEM	DRAWING AND P.C.B. MODIFICATION DESCRIPTION
ITSA-CG-98017 VER 0.1		Oct.28,98	Subject : IT8705F ADD-ON CARD APPLICATION CIRCUIT.	FIRST DRAFT
ITSA-CG-98017 VER 0.2		May.31,99	The Trace Between IT8712(Pin44) &Oscillator(output) Must Thicken and shorten. In Addition to That, The trace spacing must broaden. (SH1.SCH) ISOLATED THE VBAT & SIS960 VCCRTC (SH1.SCH) ADD JUMPER FOR FA18 & MIDI SELECTION (SH1.SCH) CIR CONNECTOR ADD OPTIONAL POWER VCCH (SH2.SCH) ADD POWER ON STRAP & FLASH ROM UP TO 4M (SH3.SCH) RN9 PIN1 CONNECT TO +3VSB (SH4.SCH) ADD MIDI FUNCTION (SH4.SCH) CHANGE R45,R48,R50 RESISTOR FROM 510 TO 51(SH5.SCH) ADD PULL UP RESISTOR R59,R60,R61 (SH5.SCH) ADD RESERVED RESISTOR R62 (SH5.SCH) CHANGE C42,C43,C44 CAP FROM 0.1UF TO 3300pF (SH5.SCH) DELETE KEYLOCK# FUNCTION (SH1.SCH & SH5.SCH) ADD LDRQ# PULL HIGH TO 3.3V 4.7K PAGE SH1 R80 FD[0..7] PULL HIGH TO 5V 8.2K PAGE SH3 RP21.RP22	
IT-8705-CG-S01 V1.1 VER 1.1		May.23,2000	ADD Smart Card Reader Function (SH1.SCH & SH4.SCH)	
IT-8705-CG-S01 V1.2 VER 1.2		Aug.22,2000	CHANGE Smart Card pin SCRPRES# Pull-up from VCCH to VCC (SH4.SCH) Add Flash ROM Pull Down Resistor (SH3.SCH)	
IT-8705-CG-S01 V1.3 VER 1.3		Mar.02,2001	Change C37 and C41 from 0.1uF to 1uF (SH5.SCH) Add VID control Circuit (SH3.SCH)	
IT-8705-CG-S01 V2.0 VER 2.0		April.26,2001	ADD Smart Card Reader Function (SH4.SCH Block E) ADD layout guideline for I/O clock(SH6.SCH)	

Preliminary

NOTE: Specification Subject to Change Without Notice.

ITE		
Title	IT8705F APPLICATION CIRCUIT	
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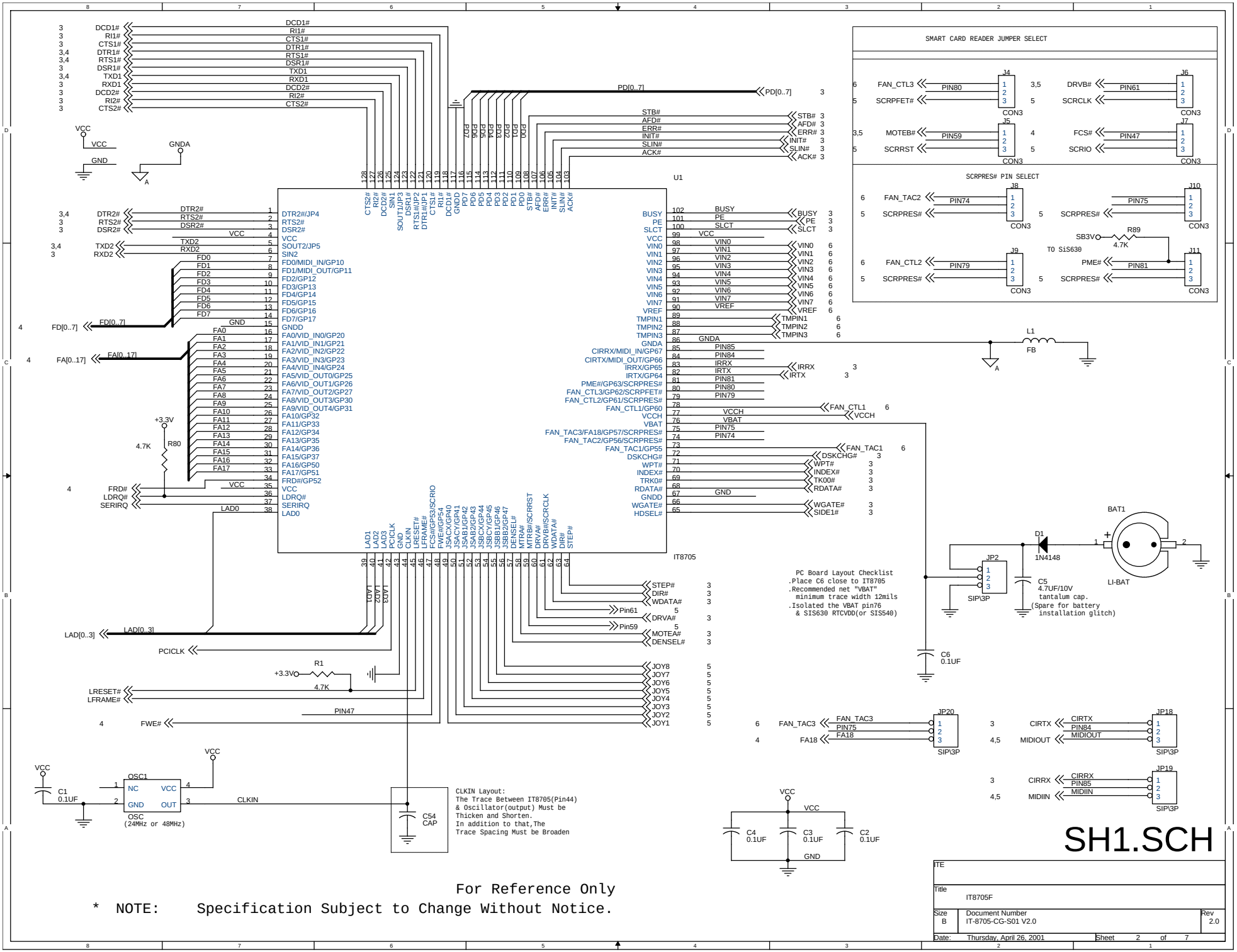
SMART CARD READER JUMPER SELECT
SCRPRES# PIN SELECT
U1
IT8705
DCD1#
RI1#
CTS1#
DTR1#
RTS1#
DSR1#
TXD1
RXD1
DCD2#
RI2#
CTS2#
PD[0..7]
STB#
AFD#
ERR#
INIT#
SLIN#
ACK#
FD[0..7]
FA[0..17]
LAD[0..3]
PCICLK
LRESET#
LFRAME#
FWE#
CLKIN
PIN47
FAN_CTL3
SCRPFET#
DRVB#
SCRCLK
MOTEB#
SCRRST
FCS#
SCRIO
FAN_TAC2
SCRPRES#
FAN_CTL2
SB3V
R89
4.7K
TO SiS630
PME#
FAN_CTL1
FAN_TAC1
BUSY
PE
SLCT
VIN0
VIN1
VIN2
VIN3
VIN4
VIN5
VIN6
VIN7
VREF
TMPIN1
TMPIN2
TMPIN3
GNDA
IRRX
IRTX
VCCH
VBAT
DSKCHG#
WPT#
INDEX#
TK00#
RDATA#
WGATE#
SIDE1#
L1
FB
BAT1
LI-BAT
D1
1N4148
JP2
SIP\3P
C5
4.7UF/10V
tantalum cap.
(Spare for battery
installation glitch)
C6
0.1UF
PC Board Layout Checklist
.Place C6 close to IT8705
.Recommended net "VBAT"
minimum trace width 12mils
.Isolated the VBAT pin76
& SIS630 RTCVDD(or SIS540)
JP20
JP18
JP19
CIRTX
CIRRX
MIDIOUT
MIDIIN
R80
R1
OSC1
OSC
(24MHz or 48MHz)
C1
0.1UF
C54
CAP
CLKIN Layout:
The Trace Between IT8705(Pin44)
& Oscillator(output) Must be
Thicken and Shorten.
In addition to that,The
Trace Spacing Must be Broaden
C4
0.1UF
C3
0.1UF
C2
0.1UF
SH1.SCH
For Reference Only
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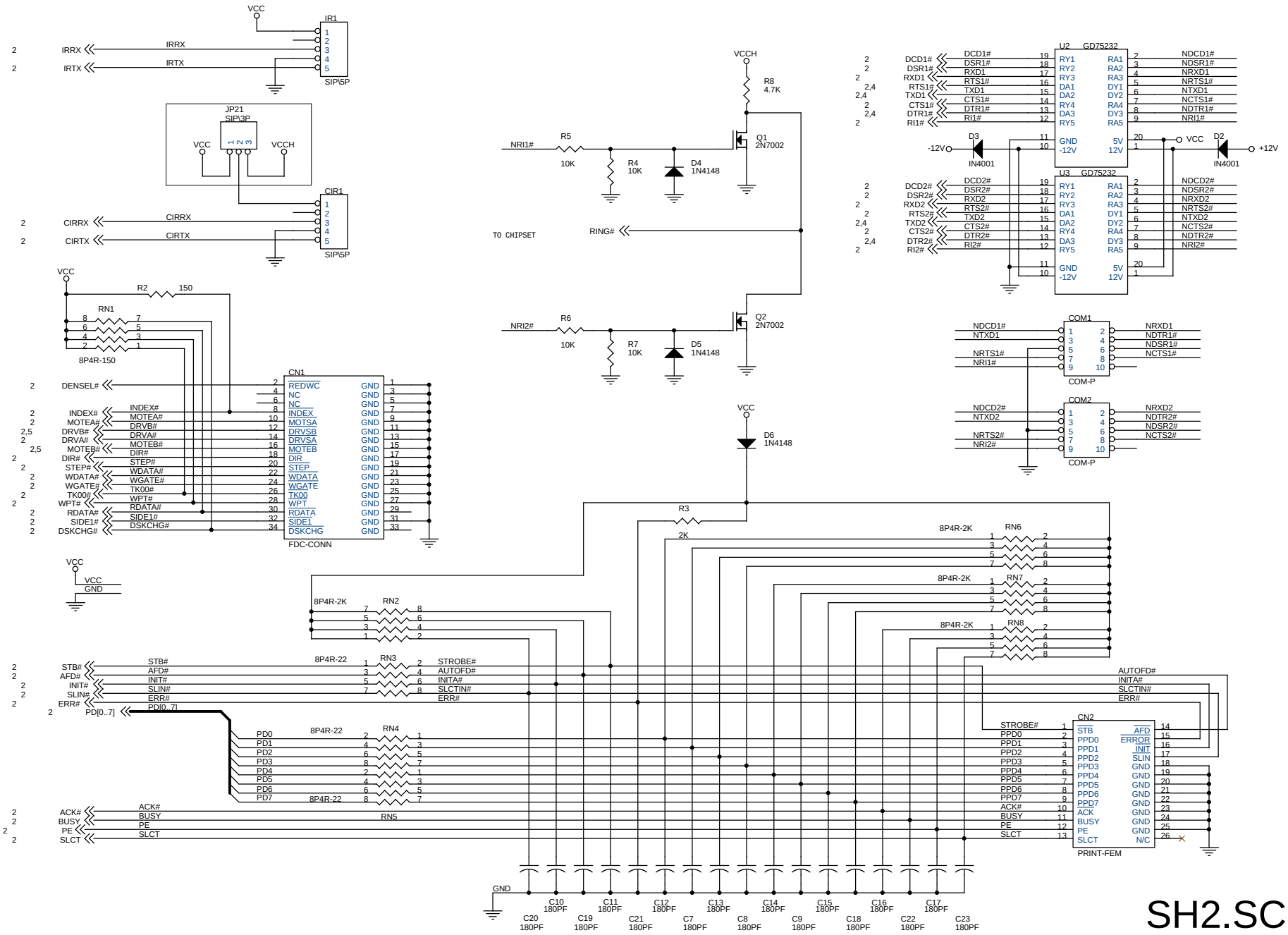

SH2.SCH

For Reference Only

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ITE		
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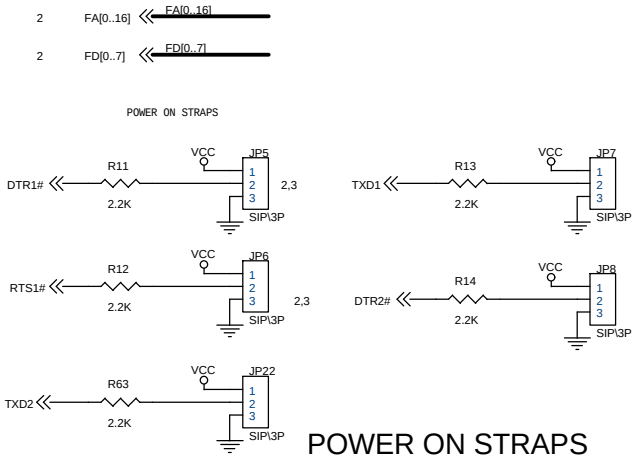


POWER ON STRAPS SETTING

	1-2 SHORT Enable FLASH ROM ADDRESS SEGMENT	2-3 SHORT DISABLE FLASH ROM
JP5	FFFF0000h~FFFFFFFFh,FFFE0000h~FFFEFFFFh	---------
JP6	FFEF0000h~FFEFFFFFh,FFEE0000h~FFEEFFFFh	---------
JP7	FFF80000h~FFFDFFFFh,FFFE0000h~FFFEFFFFh	---------
JP8	000F0000h~000FFFFFh,000E0000h~000EFFFFh	---------
JP22	ENABLE 4M FLASH ROM	---------

If select A circuit,

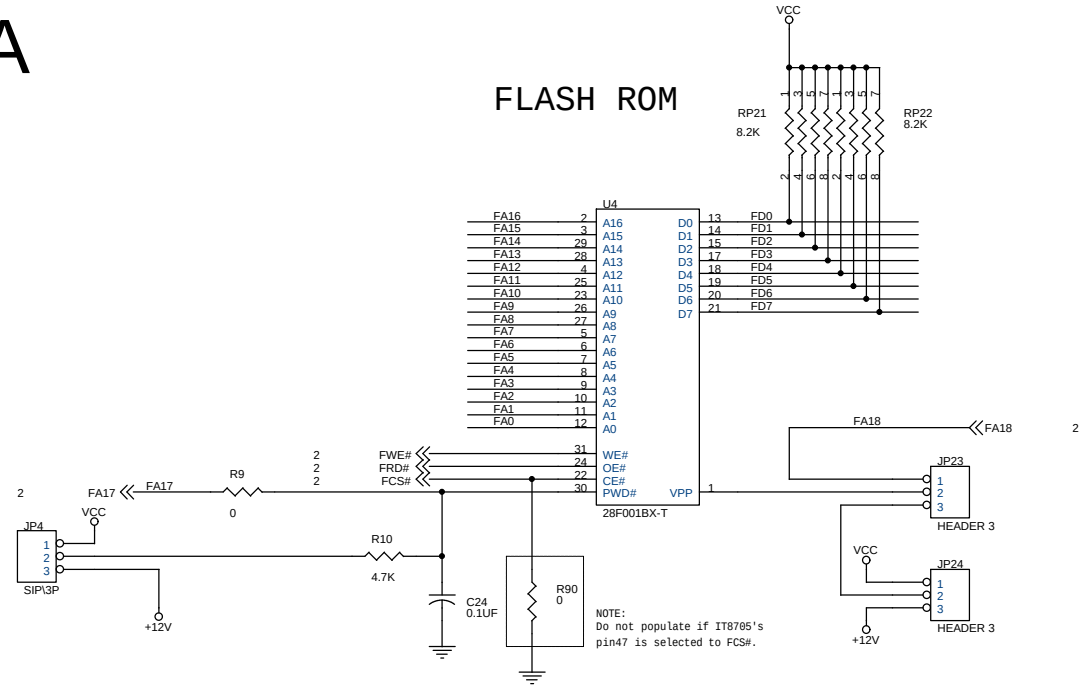
MIDIIN and MIDIOUT can not select IT8705's pin7 and pin8 .

If select B circuit,

all flash ROM interface must be disable. (JP5,JP6,JP7,JP8,JP22 Pin 2-3 short)

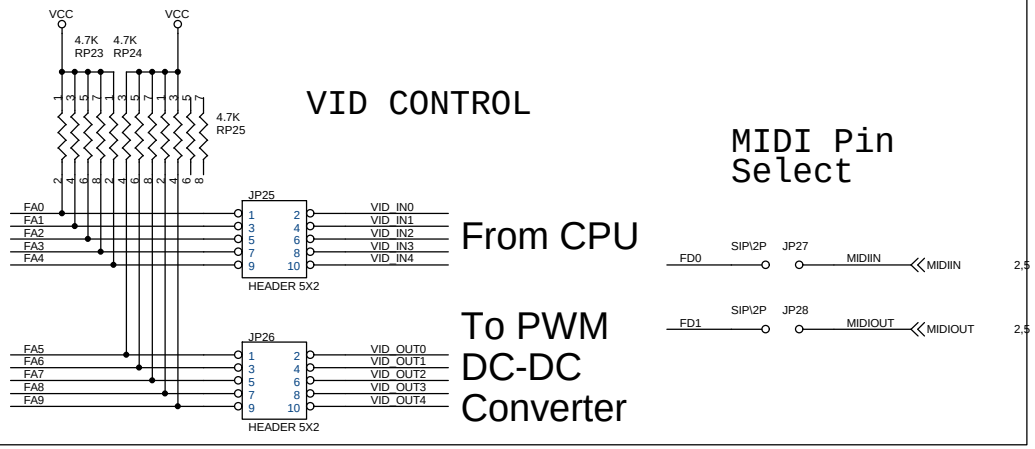
MIDIIN and MIDIOUT can select IT8705's pin7 and pin8 or others.

A



Select A or B circuit.
A and B circuit can not populate simultaneously.

B



SH3.SCH

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ITE		
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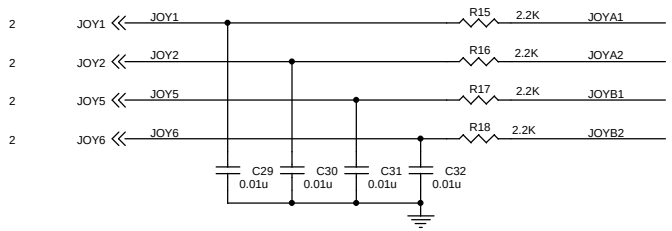
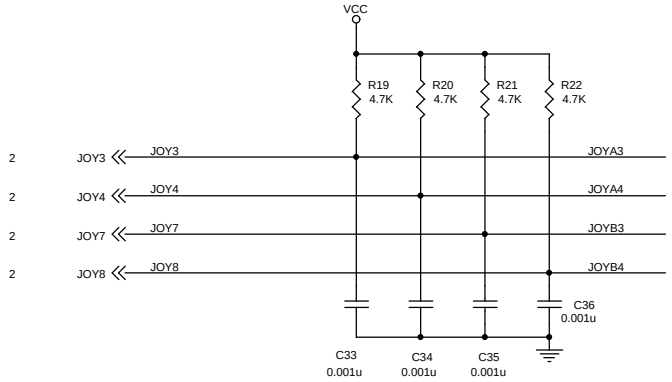
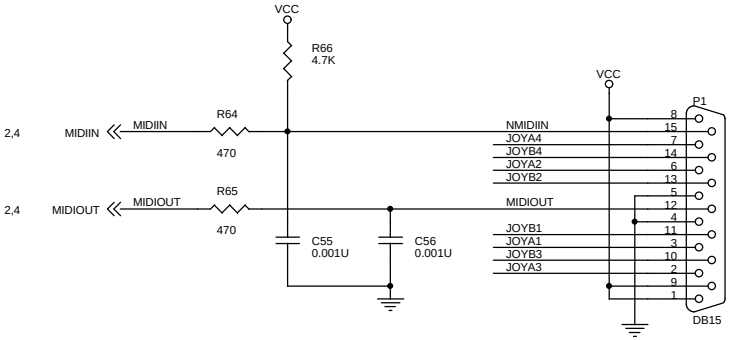
Smart Card Reader

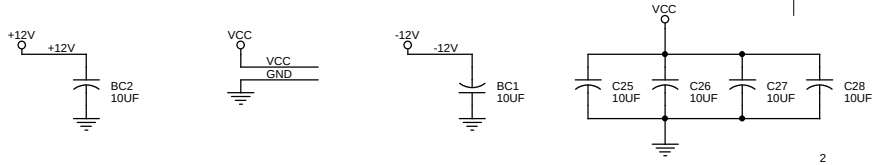
PIN TYPE MUST MATCH PHYSICAL LAYOUT



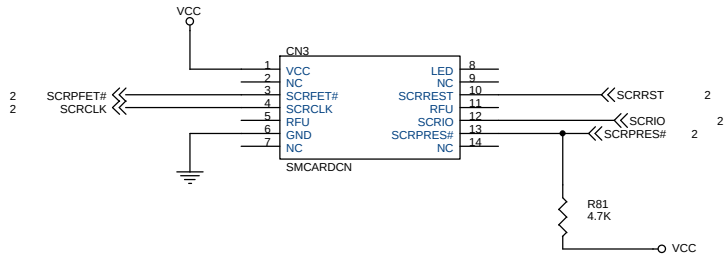




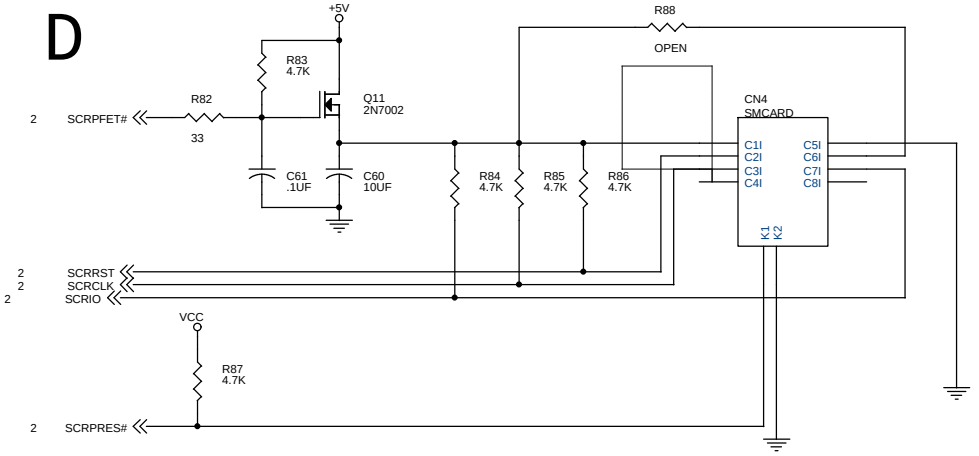
Joystick & MIDI



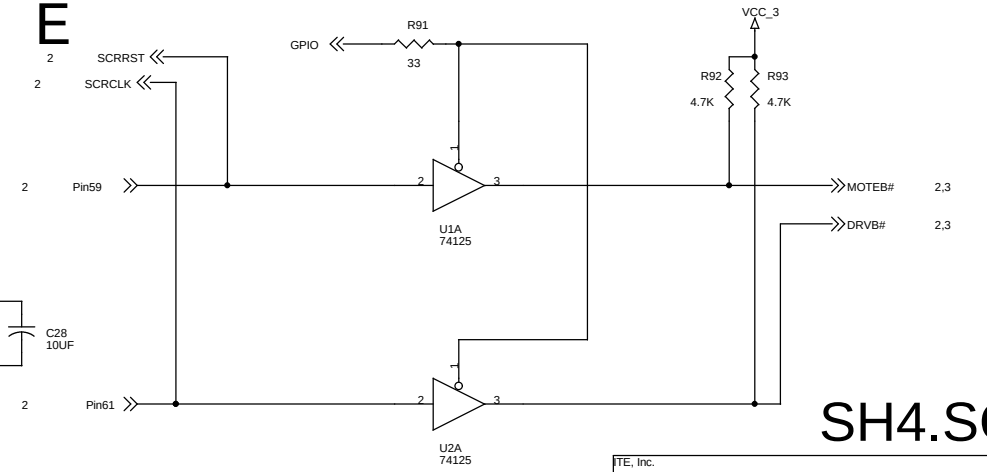
C



D



E



SH4.SCH

For Reference Only

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ITE, Inc.		
Title	Game & Smart Card Reader Connector	
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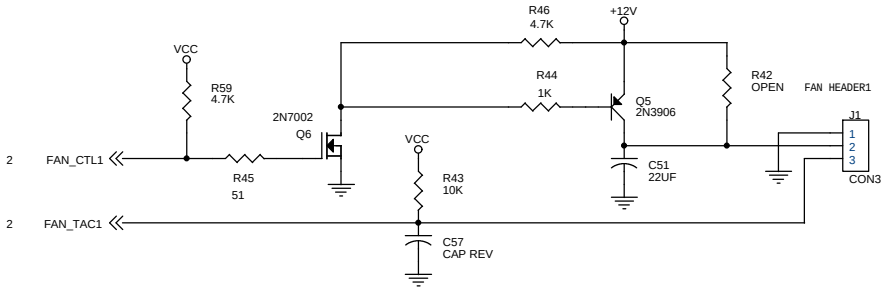
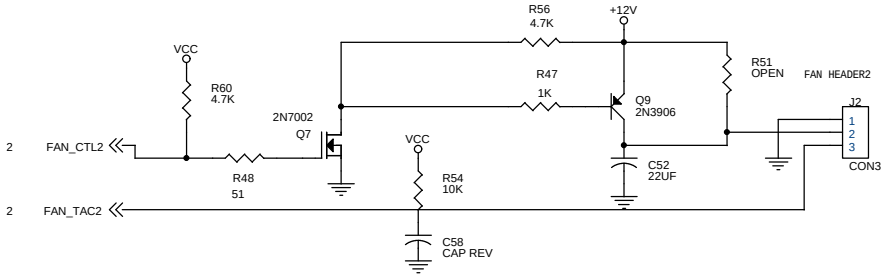
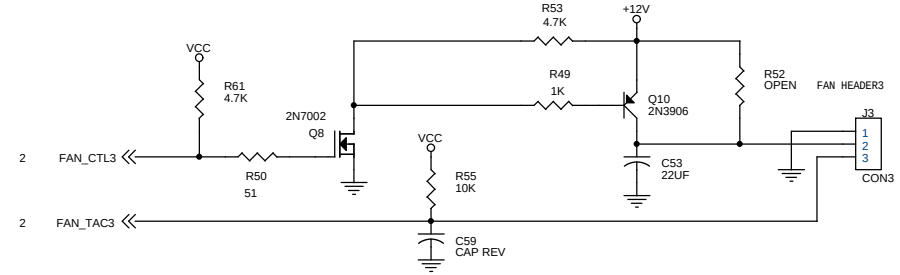
FAN Input and Output

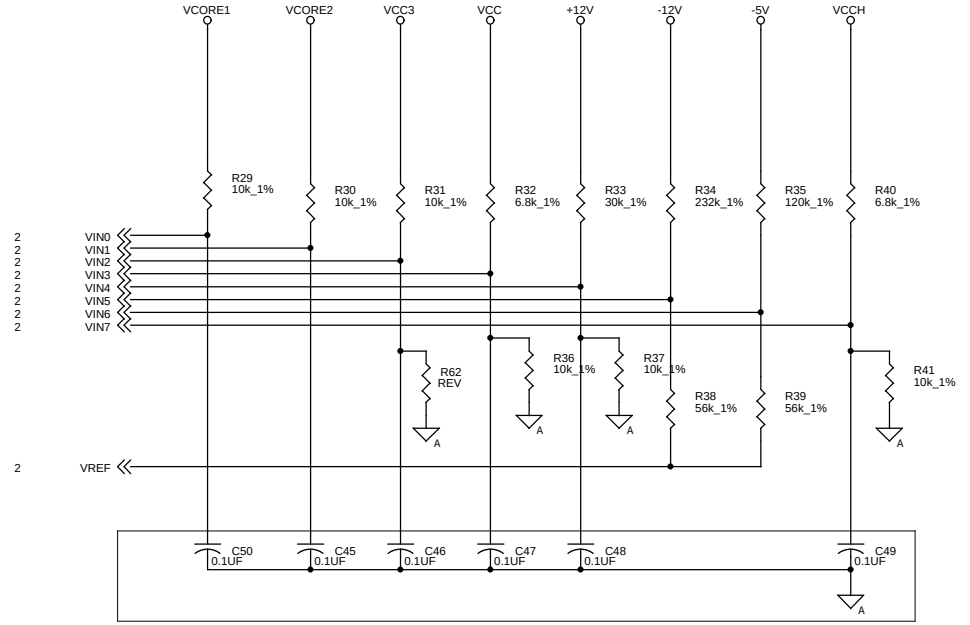




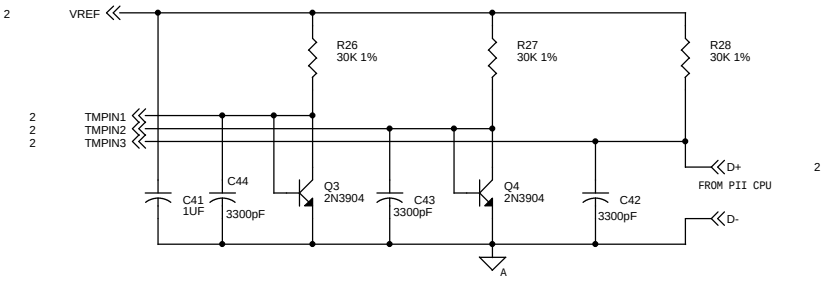


For Reference Only

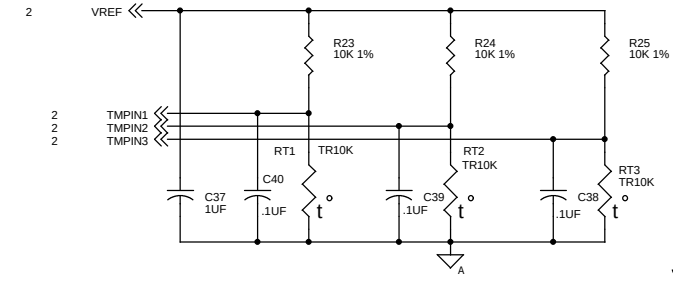
Specification Subject to Change Without Notice.

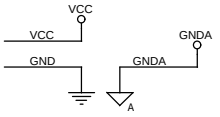


Thermal Diode layout notice:
a.Place T.D. close to IT8705F
b.Keep the trace away from: +12V, Fast data bus, CRTs.
c.Recommanded trace widths & spacings is 10 miles.



Choosing method of measuring temperature by either thermistor or diode





SH5.SCH

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LAYOUT/ROUTING GUIDELINES

1.For CLOCK LINES,

1)If possible, please avoid using any through-hole.

2)Please make the trace length short, and the trace width wide enough.

3)The spacing to the closest neighbor should be wide enough.

4)The discrete damping resistors and capacitors are recommended.

5)Please don't share I/O(24M or 48M) with other devices.

2.For the VBAT circuits,

1)Place the 1u capacitor of Vbat pin close to ITE I/O chip.

2)Vbat should be routed with a minimum trace width of 12 mils.

3)Isolate the Vbat pin of ITE I/O chipfrom the pin pinG1/VCCRTC of intel ICH with diode.

4)The 4.7u/10V tantalum capacitor connected to the diode of battery is spare for battery installation glitches.

3.Please don't remove the pull-up resistor of LDRQ#.

4.Please don't change the resistors and capacitors values in the Game and MIDI circuits.

For HARDWARE MONITOR

5.Please reserve an area for Analog Ground on your board. Moreover, connect the D- of CPU Thermal Diode and other components should be connected with AGND to this area.

6.For the temperature sensor circuits,

1)Please don't remove the 1u capacitor between Vref and AGND.

2)Place the thermal diode close to ITE I/O chip.

3)Keep the trace away from +12V, fast data bus, and CRTs.

4)Recommended trace widths and spacings are 10 mils.

5)Isolate AGND and DGND.

7.Please don't remove any components in the VINx circuits and the FANx control circuits.

8.For the SmartGuardian software compatibility,

1)Please don't change the sequence of VIN0~VIN7.

2)Please let FAN_CTL1/FAN_TAC1 circuit control and report the specific temperture which is detected by TMPIN1, let FAN_CTL2/FAN_TAC2 circuit control and report the specific temperature which is detected by TMPIN2, and let FAN_CTL3/FAN_TAC3 circuit control and report the specific temperature which is detected by TMPIN3.

9.If you would like to ignore some voltage monitoring,for example,-12V,please pull it down to GND.Don't leave it floating.

10.If the power supply is specially designed,not ATX supply,for example,every provided voltage is transferred from +12V,please note the leakage current problem caused from the standby voltages monitoring.This is due to the chip inside power plane of whole H/W Monitor is Vcc,not 5V standby.When Vcc is OFF and standby voltages are ON,the leakage will happen at the corresponding VINx pins pins from the monitored standby voltage sources.

SH6.SCH

ITE		
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