Section 2 : Pin Description

2.1 Pinout Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	AD21	AD20	AD19	AD16	IRDYJ	SERRJ	AD14	AD10	AD6	AD1	PHLDJ	GPI3	USBP1-	RTCDS	ROMKBCSJ	XD2	XD5	SD15	SD14	SD13
B	CBEJ3	AD23	AD22	AD17	FRAMEJ	STOPJ	AD15	AD11	AD7	AD2	PHLDAJ	USBCLK	USBP0+	RTCRW	XD0	XD3	XD6	SD12	DREQ7	SD11
C	AD26	AD25	AD24	AD18	CBEJ2	**DEVSELJ**	CBEJ1	AD12	CBEJ0	AD3	GPO3	GPI0	USBP0-	RTCAS	XD1	XD4	XD7	DACKJ7	SD10	DREQ6
D	AD29	AD28	AD27	AD30	AD31	TRDYJ	PAR	AD13	AD8	AD4	GPO2	SIRQI	GPO19	GPO12	GPO0	GPI2	SPKR	SD9	DACKJ6	SD8
E	PIDECS3	PIDECS1	PIDEA2	INTA	INTB	INTC	PCIRSTJ	PCICLK	AD9	AD5	AD0	USBP1+	SIRQII	GPO18	GPO9	THRMJ	SPLED	DREQ5	MEMWJ	DACKJ5
F	PIDEA0	PIDEA1	PIDEDAKJ	INTD	PIDEIRDYJ	VCC_B				**M1543**				VCC_A	VCC_E	IRQ1I	MEMRJ	DREQ0	LA17	DACKJ0
G	PIDERJ	PIDEWJ	PIDEDRQ	PIDED15	PIDED0	VCC_D									VCC3C	LA18	IRQ14	INIT	A20MJ	IRQ13
H	PIDED14	PIDED1	PIDED13	PIDED2	PIDED12			GND	GND	GND	GND	GND	GND			LA19	IRQ15	SMIJ	NMI	INTR
J	PIDED3	PIDED11	PIDED4	PIDED10	PIDED5			GND	GND	GND	GND	GND	GND			LA20	GPO20	STPCLK	IGNNEJ	CPURST
K	**PIDED9**	PIDED6	PIDED8	PIDED7	SIDECS3			GND	GND	GND	GND	GND	GND			GPO1	GPO22	RSMRSTJ	SUSTAT1J	ACPWR
L	SIDECS1	SIDEA2	SIDEA0	SIDEA1	SIDEDAKJ			GND	GND	GND	GND	GND	GND			SMBDATA	GPO23	DOCKJ	IRQ8J	PWRBTNJ
M	**SIDEIRDYJ**	SIDERJ	SIDEWJ	SIDEDRQ	SIDED15			GND	GND	GND	GND	GND	GND			SMBCLK	LA21	RI	OSC32KO	PWG
N	SIDED0	SIDED14	SIDED1	SIDED13	SIDED2			GND	GND	GND	GND	GND	GND		VDD_5S	IRQ11	LA22	IRQ10	OSC32II	OSC32I
P	SIDED12	SIDED3	SIDED11	SIDED4	XDIRJ	VCC_A_D									VCC_C	LA23	IO16	SBHEJ	M16	OSC14M
R	SIDED10	SIDED5	SIDED9	XMOT1J	XDRV0J	VDD_5	VCC_A_D							VCC_3A	VCC_A	BALE	TC	SA0	SA1	SA2
T	SIDED6	SIDED8	XDSKCHGJ	XDRV1J	XMOT0J	XDENSEL	XDCD1J	XPD3	XACKJ	RSTDRV	MSCLK	MSDATA	SD0	SA19	DACKJ3	DACKJ2	SA6	SA3	SA4	SA5
U	SIDED7	XHDSELJ	XRDATAJ	XINDEXJ	XDCD2J	XDSR1J	XSTROBJ	XPD4	XBUSY	XERRORJ	KBCLK	KBDATA	SD1	SMEMRJ	SA17	IRQ3	IRQ5	SA8	SA7	IRQ4
V	XWPROTJ	XTRK0J	XWGATEJ	XDTR2J	XRI1J	XDTR1J	XPD0	XPD5	XPE	XINITJ	IRQ9	DREQ2	NOWSJ	AEN	IORJ	SA15	DREQ1	SA10	IRQ6	SA9
W	XWDATAJ	XSTEPJ	XRTS2J	XSOUT2	XCTS1J	XSOUT1	XPD1	XPD6	XSLCT	XSLCTINJ	SD6	SD4	SD2	SMEMWJ	SA18	DREQ3	SA14	SYSCLK	SA11	IRQ7
Y	XRI2J	XCTS2J	XDSR2J	XSIN2	XRTS1J	XSIN1	XPD2	XPD7	XAUTOFDJ	IOCK	SD7	SD5	SD3	IOCHRDY	IOWJ	SA16	DACKJ1	SA13	REFRSHJ	SA12

Figure 2-1. Pinout Diagram

Note : Please refer to p.199 for bottom view

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2.2 Pin Description Table :

Pin Name	Type	Description
Clock & Reset Interface :		
PWG	I Group C Schmitt	**Power-Good Input.** This signal comes from the power supply to indicate that power is available and stable. The de-assertion of this input will enable the leakage control circuit between Soft-off (Suspend to Disk) resume circuit and no power circuit.
PCICLK	I Group B	**PCI Clock for Internal PCI Interface.** This is an input PCI clock, it should always be running at ON, STANDBY, SLEEP (Power-On Suspend) state. When CLKRUNJ is active, this clock should always be running. Internal PCI state machine and ISA state machine will use this clock.
OSC14M	I Group A	**14.318Mhz Clock Input.** This input clock will be used for Power Management timer, M8254 timer, SM Bus base frequency and ISA state machine.
OSC32KI	I Group C	**32 KHz Oscillator Input 1.** This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The M1543 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, an external 32 Khz clock input should be connected to this pin.
OSC32KII	I Group C	**32 KHz Oscillator Input2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The M1543 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, this pin should be floated.
CLK32KO	O Group C 2.4/2.4 mA	**32 KHz Clock Output for DRAM Refresh.** At ON, STANDBY, SLEEP (Power On Suspend), SUSPEND (Suspend to DRAM) states, the output will send to Memory controller, to support DRAM refresh clock. At Soft off and Suspend to Disk states, the output will drive low to avoid leakage current.
USBCLK	I Group B	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
PCI Bus Interface :		
PCIRSTJ	O-Group B 12/16 mA	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.
AD[31:0]	I/O Group B 12/16 mA	**Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBEJ[3:0]	I/O-Group B 12/16 mA	**Bus Command and Byte Enable.** During address phase, CBEJ[3:0] define the Bus Command. During the data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	I/O -Group B 12/16 mA	**Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.
TRDYJ	I/O -Group B 12/16 mA	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
IRDYJ	I/O-Group B 12/16 mA	**Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
STOPJ	I/O-Group B 12/16 mA	**Cycle Stop Request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
DEVSELJ	I/O Group B 12/16 mA	**Device Select.** This signal indicates that the target device has decoded the address as its own cycle. This pin is an output pin when M1543 acts as a PCI slave has decoded address as its own cycle including subtractive decoding.
SERRJ	I -Group B	**System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERRJ is sampling low, M1543 will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O Group B 12/16 mA	**Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBEJ[3:0]. When M1543 acts as a PCI master, it drives PAR one PCI clock after address phase for read/write transaction and one PCI clock after data phase for write transaction. When the M1543 acts as a target, it drives PAR one PCI clock after data phase for PCI master read transaction.

Pin Description Table (continued) :

Pin Name	Type	Description
PCI Bus Interface :		
PHLDAJ	I Group B	**PCI Bus Ownership Acknowledge.** When PCI bus arbiter asserts this pin, M1543 has owned the PCI bus.
PHOLDJ	O-Group B 4/4 mA	**PCI Bus Ownership Request.** M1543 requests the ownership of the PCI bus from the PCI bus arbiter on the North Bridge. M1543 will assert this signal on behalf of the ISA Master, DMA Device, IDE Master, and the USB Master.
INTAJ_MI	I Group B	**PCI INTA.** PCI interrupt input A or PCI interrupt polling input. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTAJ when 4 PCI Interrupts are supported, or connects to the 74F181 encoded output to support the 8 PCI Interrupts polling mode.
INTBJS0	I/O Group B Schmitt 4/4 mA	**PCI INTB.** PCI interrupt input B or polling select_0 output. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTBJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 0 to support the 8 PCI Interrupts polling mode.
INTCJS1	I/O Group B Schmitt 4/4 mA	**PCI INTC.** PCI interrupt input C or polling select_1 output. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTCJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 1 to support the 8 PCI Interrupts polling mode.
INTDJS2	I/O Group B Schmitt 4/4 mA	**PCI INTD.** PCI interrupt input D or polling select_2 output. M1543 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTDJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 2 to support the 8 PCI Interrupts polling mode.
CPU interface :		
INIT	O-Group E 2.4/2.4 mA	**CPU Initialize Interrupt.** CPU cold & warm reset. When CPU is Pentium Pro, this signal is low active. Otherwise, this signal is high active. When power on, KBC RC, port 92 RC, shutting down all will trigger INIT active.
CPURST	O-Group E 2.4/2.4 mA	**CPU Cold Reset.** When power turn on, this reset signal will be asserted, and then will become de-asserted until 4 ms after PWG becomes high.
IGNNEJ	O-Group E 2.4/2.4 mA	**Ignore Error.** This pin is used as the ignore numeric coprocessor error.
INTR	O-Group E 2.4/2.4 mA	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt.
NMI	O Group E 2.4/2.4 mA	**Non-maskable Interrupt to CPU.** This is generated by the ISA Parity error (IOCHKJ assertion), PCI Parity error or DRAM Parity error (SERRJ assertion), and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt.
A20MJ	O-Group E 2.4/2.4 mA	**CPU A20 Mask.** This is the CPU Address line A20 mask signal.
FERRJ/ IRQ13	I Group E	**Floating Point Error.** FERRJ input to generate IRQ13. When coprocessor interface is disabled through configuration register Index-43h bit 6 setting, the function of this pin is IRQ13.
ISA Bus Interface :		
IRQ[15:14], IRQ[11:9], IRQ[7:3]	I/O Group A Schmitt 9.6/9.6 mA	**Interrupt Request.** The Interrupt Request lines are directly from the ISA Bus, from the PCI Interrupt Routing, or from the steerable Interrupt pins. The M1543 will also drive the interrupt pins if the source is not from the ISA bus to support the APIC interface.
RSTDRV	O-Group A 12/16mA	**ISA Bus Reset.** This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.
SD[15:8]	I/O-Group A 12/12 mA	**ISA High Byte Slot Data Bus.** These pins should connect to the ISA High Byte Slot Data Bus.

Pin Description Table (continued) :

Pin Name	Type	Description
ISA Bus Interface :		
XD[7:0]	I/O Group A 12/12 mA	**XD Data Bus.** When the SD[7:0] pins are defined as GPIO[7:0] pins, these pins can be used to drive SD[7:0] if TTL LS245 is used as a buffer. The M1543 signal XDIR will control this buffer.
SD[7:0]/ GPIO[7:0]	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus or General Purpose I/O.** When external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL, these pins are used as the GPIO pins for green control. Otherwise, these pins are SD[7:0]. No external LS245 is required.
SA[19:17]	O-Group A 12/12 mA	**ISA Slot Address Bus A19-A17.** These pins should connect to the ISA System Address Bus.
SA[16:0]	I/O-Group A 12/12 mA	**ISA Slot Address Bus A16-A0.** These pins should connect to the ISA System Address Bus.
SBHEJ	I/O -Group A 12/12 mA	**ISA Byte High Enable.** This pin should connect to the ISA System Byte High Enable pin.
LA[23:17]	I/O-Group A 12/12 mA	**ISA Latched Address Bus.** They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.
IO16J	I -Group A	**ISA 16 Bit I/O Device Indicator.** This is an input and will be driven by the device if the ISA I/O cycle is a 16-bit access.
M16J	I/O-Group A 12/20 mA	**ISA 16 Bit Memory Device Indicator.** This pin will be driven by the device or by the M1543 if the ISA Memory cycle is a 16-bit access.
MEMRJ	I/O-Group A 12/12 mA	**ISA Memory Read.** This signal is an output when the M1543 is the ISA Bus master, or an input during ISA master cycle.
MEMWJ	I/O -Group A 12/12 mA	**ISA Memory Write.** This signal is an output when the M1543 is the ISA Bus master, or an input during ISA master cycle.
AEN	O-Group A 12/12 mA	**ISA I/O Address Enable.** This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.
IOCHRDY	I/O-Group A 12/20 mA	**ISA System Ready.** This signal is an output during ISA master cycle, or an input when the M1543 is the ISA Bus master .
NOWSJ	I-Group A	**ISA Zero Wait-State for Input.** This input signal will terminate the CPU to ISA command instantly.
IOCHKJ	I-Group A	**ISA Parity Error.** M1543 will generate NMI to CPU when this signal is asserted.
SYSCLK	O-Group A 12/12 mA	**ISA System Clock.** This output is generated by the PCI clock and is used as the ISA system clock.
BALE	O-Group A 12/12 mA	**Bus Address Latch Enable.** BALE will be asserted throughout DMA, ISA master, and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.
IORJ	I/O-Group A 12/16 mA	**ISA I/O Read.** This signal is an input during ISA master cycle, and an output when the M1543 is the ISA Bus master.
IOWJ	I/O-Group A 12/12 mA	**ISA I/O write.** This signal is an input during ISA master cycle, and an output when the M1543 is the ISA Bus master.
SMEMRJ	O-Group A 12/12 mA	**ISA System Memory Read.** This signal indicates that the memory read command is below 1M Byte address.
SMEMWJ	O-Group A 12/12 mA	**ISA System Memory Write.** This signal indicates that the memory write command is below 1M Byte address.
DREQ[7:5], DREQ[3:0]	I-Group A Schmitt	**DMA Request Signals.** These are inputs from the DMA Device or ISA Master Request. The M1543 will combine the DMA request, ISA Master request, IDE Bus Master request, and USB Master request to generate the PHOLDJ to the PCI Arbiter.
DACKJ[7:5], DACKJ[3:0]	O-Group A 9.6/9.6 mA	**DMA Acknowledge Signals.** After the M1543 has acquired the PCI Bus grant (PHLDAJ), the internal arbiter will assert the DMA acknowledge signal to the DMA Device Request.

Pin Description Table (continued) :

Pin Name	Type	Description
ISA Bus Interface :		
TC	O-Group A	**DMA End of Process.** This signal will be asserted after the DMA Device has ended the transaction.
REFRSHJ	I/O Group A	**ISA Refresh Cycle.** This signal is an input during ISA master cycle, and an output when the M1543 is the ISA Bus master.
Miscellaneous Logic :		
SPKR	O-Group A	**Speaker Output.** This pin is used to control the Speaker Output and should connect to the Speaker.
RTCAS	O-Group A	**RTC Address Strobe.** This pin is used as the RTC Address Strobe and should connect to the RTC.
RTCRW	O-Group A	**RTC Write Strobe.** This pin is used as the RTC Read/Write Command and should connect to the RTC. The M1543 will drive the RTC command through dedicated pin instead of the 74F32 decode to save the system cost.
RTCDS	O-Group A	**RTC Data Strobe.** This pin is used as the RTC Data Strobe and should connect to the RTC.
SPLED	O-Group A	**Speed LED Output.** This pin is used to control the Speed LED Output and should connect to LED.
ROMKBCSJ	O-Group A	**ROM/Keyboard Chip Select.** This pin is the ROM chip select and is the Keyboard chip select also when internal KBC is disabled.
SERIRQ/ GPI[2]	B/I Group A	**Serial Interrupt Request or General Purpose Input.** This pin is used to support the serial interrupt protocol or as a General Purpose Input.
SIRQI	I -Group A	**Steerable IRQ Input1.** This is a steerable Interrupt input, M1543 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
SIRQII	I -Group A	**Steerable IRQ Input2.** This is a steerable Interrupt input, M1543 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
IRQ8J	I -Group C	**RTC Interrupt Input.** This is the RTC Interrupt input. This pin belongs to the Power Group C, and it can support the RTC Alarm function during Soft-off or Suspend state.
XDIR/ GPO[12]	O-Group A	**XD Bus Direction Control or General Purpose Output.** When external XD bus is designed on motherboard, this pin is X-bus direction control. Otherwise, this pin is a general purpose output.
KBINH/ IRQ1I	I/O Group A	**Keyboard Inhibit or Interrupt One Input.** This pin will be the Keyboard Inhibit input when internal KBC is enabled. Otherwise, it will be the IRQ1 input.
KBCLK/ GPI[9]	I/O Group A	**Keyboard Clock or General Purpose Input.** This pin is the Keyboard interface Clock when internal KBC is enabled. Otherwise, it is a general purpose input.
KBDATA/ GPI[10]	I/O Group A	**Keyboard data or General Purpose Input.** KB interface DATA output when internal KBC is enabled. Otherwise, this pin is a general purpose input.
MSCLK/ GPI[11]	I/O Group A	**Mouse Clock or General Purpose Input.** Mouse clock output when internal PS2 Keyboard is enabled. Otherwise, this pin is a general purpose input.
MDATA/ IRQ12I	I/O Group A	**Mouse Data or Interrupt Line 12 Input.** Mouse data output when internal PS2 Keyboard is enabled. Otherwise, this pin is the IRQ12 input.
BIOSA17/ GPO[19]	O-Group A	**ROM Address 17 or General Purpose Output.** This pin is the ROM A17 control when 2M ROM is used, or it is a general purpose output.
BIOSA16/ GPO[18]	O-Group A	**ROM Address 17 or General Purpose Output.** This pin is the ROM A16 control when 2M ROM is used, or it is a general purpose output.
PCSJ/ GPO[0]	O-Group A	**Programmable Chip Select or General Purpose Output.** This pin can be selected as a programmable Chip Select, or as a general purpose output.
IDE interface :		
PIDE_DRQ	I-Group D	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer.
SIDE_DRQ	I-Group D	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer.

Pin Description Table (continued) :

Pin Name	Type	Description
IDE interface :		
PIDE_AKJ	O-Group D	**Primary IDE DACKJ for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer.
SIDE_AKJ	O-Group D	**Secondary IDE DACKJ for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer.
PIDE_RDY	I-Group D	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
SIDE_RDY	I-Group D	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
PIDEIORJ	O-Group D	**Primary IDE IORJ Command.** This is the IORJ command output pin to notify the Primary IDE device to assert the Read Data.
SIDEIORJ	O-Group D	**Secondary IDE IORJ Command.** This is the IORJ command output pin to notify the Secondary IDE device to assert the Read Data.
PIDEIOWJ	O-Group D	**Primary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Primary IDE device that the available Write Data is already asserted by M1543.
SIDEIOWJ	O-Group D	**Secondary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Secondary IDE device that the available Write Data is already asserted by M1543.
PIDECS1J	O-Group D	**IDE Chip Select 1 for Secondary Channel 0.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3J	O-Group D	**IDE Chip Select 3 for Secondary Channel 1.** This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
SIDECS1J	O-Group D	**IDE Chip Select 1 for Primary Channel 0.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3J	O-Group D	**IDE Chip Select 3 for Primary Channel 1.** This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
PIDE_A[2:0]	O-Group D	**Primary IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
SIDE_A[2:0]	O-Group D	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
PIDE_D[15:0]	I/O Group D	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
SIDE_D[15:0]	I/O Group D	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
Power Management Unit :		
RSM_RSTJ	I-Group C Schmitt	**Resume Circuit Initial Reset Input.** This input is used to initialize the resume circuit.
SMIJ	O-Group E 4/4 mA	**SMM Interrupt Output.** This output should be connected to CPU SMM Interrupt input.
STPCLKJ	O-Group E 4/4 mA	**Stop CPU Internal Clock Output.** This output is used to stop the CPU internal clock and should be connected to CPU STPCLKJ input.
SLEEPJ/ GPO[20]	O-Group E 4/4 mA	**Pentium PRO Sleep State or General Purpose Output.** This output will force Pentium PRO CPU to enter Sleep State, or as a general purpose output.

Pin Description Table (continued) :

Pin Name	Type	Description
Power Management Unit :		
ZZ/ GPO[1]	O-Group E 4/4mA	**PBSRAM Power Saving Mode or General Purpose Output.** This output is used to control L2 cache entering power saving mode, or as a general purpose output.
CPU_STPJ/ GPO[2]	O-Group B 4/4mA	**Clock Cell CPU Clock Stop or General Purpose Output.** This output is used to stop the CPU Clock of the clock generator, or as a general purpose output.
PCI_STPJ/ GPO[3]	O-Group B 4/4mA	**Clock Cell PCI Clock Stop or General Purpose Output.** This output is used to stop the PCI Clock of the clock generator, or as a general purpose output.
SUSTAT1J	O-Group C 4/4 mA	**Suspend Status for North Bridge.** This output is used to notice the north bridge to control DRAM suspend refresh circuit.
PWRBTNJ	I-Group C Schmitt	**Power Button Input.** This input is used to support the ACPI Power Button function.
PCIREQJ/ GPI[3]	I-Group B	**PCI Bus Request Event Input or General Purpose Input.** This input comes from the North Bridge or external circuit to notice M1543 there is PCI request pending. This pin can also be programmed as a general purpose input.
SQWO/ GPO[9]	O-Group A 4/4mA	**Square Wave Output or General Purpose Output.** This output can be used to output Square Wave with 1Hz or 2Hz, or as a general purpose output.
OFF_PWR1/ GPO[22]	O-Group C 4/4mA	**Remove All Circuit Power Except Internal Suspend Circuit and External DRAM or General Purpose Output.**
OFF_PWR2/ GPO[23]	O-Group C 4/4mA	**Remove All Circuit Power Except Internal Suspend Circuit or General Purpose Output.**
RI	I-Group C Schmitt	**Ring-in or General Purpose Input.** This input connects to Modem Ring-in input to support ACPI Ring-in function, or as a general purpose input.
THRMJ	I-Group A Schmitt	**Thermal Event Input or General Purpose Input.** THRMJ is a triggered input to the M1543 showing that the external thermal detected circuits are requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
ACPWR	I-Group A Schmitt	**Detect AC Adapter Plug-in or General Purpose Input.** This is a triggered input showing that the AC adapter is plugged in or plugged out event. This triggered event can be used as a system management (or control) interrupt source. This signal also can be used optionally as a general purpose input signal.
DOCKJ	I-Group C	**Docking Insert Event Input or General Purpose Input.** This triggered input is used as a docking event indicator, or as a general purpose input signal.
USB interface :		
USBP0+ USBP0-	I/O Group B	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USBP1+ USBP1-	I/O Group B	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
OVCRJ/ GPI[0]	I Group B	**Over Current Detect Inputs or General Purpose Input.** This pin is used to monitor the USB Power Over Current, or as a general purpose input.
SM Bus signal :		
SMBCLK	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Clock.** SM Bus clock signal should be combined with SM Bus data to carry information between the devices connected to the SM Bus.
SMBDATA	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Data Line.** SM Bus data signal should be combined with SM Bus clock to carry information between the devices connected to the SM Bus.

Pin Description Table (continued) :

Pin Name	Type	Description
Floppy Disk Interface :		
RDATAJ	I (IS) Group A	**Read Disk Data.** The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	O (O36) Group A	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
WDATAJ	O (O36) Group A	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	O (O36) Group A	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	O (O36) Group A	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
STEPJ	O (O36) Group A	**Step.** This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
DSKCHGJ	I (IS) Group A	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
DRV0J, DRV1J	O (O36) Group A	**Drive Select 0, 1**. Active low, output select drives 0-1.
MOT0J, MOT1J	O (O36) Group A	**Motor on 0, 1**. These active-low outputs select motor drives 0-1.
WPROTJ	I (IS) Group A	**Write Protected**. This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.
TRK0J	I (IS) Group A	**Track 00**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	I (IS) Group A	**Index**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
DENSEL	O (O36) Group A	**Density Select**. Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.
Serial Port Interface :		
SIN1, SIN2	I (IS) Group A	**Receive Data**. Receiver serial data input signal.
SOUT1, SOUT2	O (O4) Group A	**Transmit Data**. Transmitter serial data output from Serial Port.
RTS1J	O (O4) Group A	**Request to send**. Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
CFGPORT	I Group A	**Configuration port select**. During reset active, this input is read and latched to define the configuration register's base address. This pin has a 20K(default) internal pull-up resistor.
RTS2J	O (O4) Group A	**Request to send**. This active low output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
KBC_EN	I Group A	**KBC enable control**. During reset active, this input is read and latched to enable KBC after reset. The enable could be overwritten by configuration register. This pin has a 20K(default) internal pull-up resistor.

Pin Description Table (continued) :

Pin Name	Type	Description
Serial Port Interface :		
DTR1J	O (O4) Group A	**Data Terminal Ready**. This is an active low output for primary serial port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation.
FULLDEC	I Group A	**Full decoder enable.** During reset active, this input is read and latched to determine whether a fully decoder (SA15-SA11) is supported. This pin has a 20K(default) internal pull-up resistor.
DTR2J	O (O4) Group A	**Data Terminal Ready.** This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation.
PS2_ATJ	I Group A	**KBC PS2 mode or AT mode select.** When active, this input is read and latched to define the KBC PS-2 or AT mode. This pin has a 20K(default) internal pull-up resistor.
CTS1J CTS2J	I (IS) Group A	**Clear to Send.** This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	I (IS) Group A	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	I (IS) Group A	**Data Carrier Detect**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. Note : bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	I (IS) Group A	**Ring Indicator**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note : bit 6 of MSR is the complement of RIJ.
Printer Port Interface :		
AUTOFDJ	O (O20) Group A	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
INITJ	O (O20) Group A	**Initiate Output**. This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
SLCTINJ	O (O20) Group A	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.

Pin Description Table (continued) :

Pin Name	Type	Description
Printer Port Interface :		
STROBJ	O (O20) Group A	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	I (IS) Group A	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	I (IS) Group A	**Acknowledge**. This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	I (IS) Group A	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	I (IS) Group A	**Printer Selected Status**. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	O (O20) Group A	**Error**. This active low signal indicates an error condition at the printer.
PD0-PD7	I/O (I/O20) Group A	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
Power Pins :		
VCC_A	P	**Vcc for Power Group A.** This power is used for ISA interface.
VCC_3A	P	**Vcc for Power Group A.** This power is used for ISA interface.
VCC_B	P	**Vcc for Power Group B.** This power is used for PCI interface.
VCC_C	P	**Vcc for Power Group C.** This power is used for resume/suspend control interface signals during normal operation and suspend periods.
VCC_3C	P	**Vcc for Power Group C.** This power is used for Resume/Suspend Control interface.
VCC_D	P	**Vcc for Power Group D.** This power is used for IDE interface.
VCC_E	P	**Vcc 3.3V or 2.5V for Power Group E.** This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_5	P	**Vcc 5.0V for core Power.** It supplies the core power for the internal circuit except the suspend circuit.
VDD_5S	P	**Vcc 5.0V for Suspend/Resume Core Power.** It supplies the core power for the internal suspend/resume circuit.
Vss or Gnd	P	**Ground.**

Type Description :

I	Input TTL compatible.
IS	Input with Schmitt Trigger.
I/O16	Input/Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
I/O20	Input/Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V.
ICLK	CLK input.
OCLK	CLK output.
O4	Output with 4 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
O8	Output with 8 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
O16	Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
O20	Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V.
O36	Output with 36 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
OD16	Open drain outputs, sinks 24 mA @ 0.4 V.