2.2 Pin Description

Table 2-1 lists the functions of all M5115 pins. A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Table 2-1 M5115 Pin Description Table

Name	Number	Type	Drive Strength*	Description
				Floppy Disk Controller
-ACK	31	I		**Acknowledge.** When set low by the printer, this input indicates that the printer has received data.
-DAK2	70	I		**DMA Acknowledge.** This is an active-low input used to acknowledge DMA requests, and to enable the -RD and -WR inputs. This signal is enabled when D3 of the drive control register is set.
DIR	91	O	48 mA*	**Direction.** This high-drive, open-drain output determines the direction of the head movement (low = step-in, high = step-out). When in the write or read modes, this output is high.
-DR0, -DR1	93, 92	O	48 mA*	**Drive.** These high-drive, open-drain outputs are drive-select signals for drives 0 and 1. They are ANDed with the corresponding motor enable lines. These pins contain encoded drive-select information if bit 7 of the configuration register is set.
DRQ2	69	O	10.7 mA*	**DMA Request.** This is an active-high output that signals the DMA controller that a data transfer is needed. It is enabled when D3 of the drive control register is set.
-U2ENABLE	84	O		**IDE High Byte Enable.** This signal is active-low only in AT mode. The I/O address for this pin reacts are 1F0H - 1F7H in primary address mode.
DSKCHG/RG	73	I		**Disk Change/Read Gate.** This disk interface input indicates when the disk drive door has been opened. The active-high state of this input is read from bit D7 of address xx7h. When RG bit in the mode command is set, this pin functions as a read-gate signal. When low, it forces the data separator to lock to the crystal, and when high it locks to the data for diagnostic purposes.
FILTER	82	I/O		**Filter.** This pin is the output of the charge pump and the input to the VCO. One or more filters are attached between this pin and the FGND250, FGND500, and VSSA pins.
-U1ENABLE	80	O		**IDE Low Signal Byte.** This low-signal byte is used in AT mode. This pin is active when the IDE is enabled and the I/O address is accessing 1F0H-1F7H and 3F6-3F7* in primary address mode.
HDSEL	96	O	40 mA*	**Head Select.** This high-drive, open-drain output determines which disk drive head is active. Low = Head 1, high (open) = Head 0.
-INDEX	98	I		**Index.** This pin signals the beginning of a track.

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Table 2-1 M5115 Pin Description Table (continued)

Name	Number	Type	Drive Strength*	Description
			Floppy Disk Controller	
IRQ6	72	O	12 mA*	**Interrupt Request 6.** This signals that a flexible-disk controller operation requires the attention of the microprocessor. The action required depends on the current function of the controller. This signal is enabled when D3 of the drive control register is set.
-MTR0, -MTR1	95, 94	O	48mA*	**Motors.** These high-drive, open-drain outputs are motor enable signals for drives 0 and 1. These pins contain encoded drive select information if bit 7 of the configuration register is set. Otherwise they are controlled through bits in the drive control register.
-RDATA	78	I		**Read Data.** The active-low, raw data read from the disk is connected here.
RPM/LC	88	O	6mA*	**Density Select**. Indicates whether a low (250/300 Kbps) or high (500 Kbps/1Mbps) data rate has been selected.
SETCUR	85	O		**Set Current.** An external resistor connected from this pin to analog ground programs the amount of charge pump current that drives the external filters. The 4.5.1.4 PLL Filter Design section shows how to determine the values. A standard value at this pin is 8.2K ~ 10K.
-WDATA	90	O	48mA*	**Write Data.** This high-drive, open-drain output is a write-precompensated serial data to be written onto the selected disk drive.
-WGATE	86	O	48mA*	**Write Gate.** This active-low, open-drain, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
-WPROT	99	I		**Write Protect.** This input indicates that the disk is write-protected. When a disk is write-protected, any command that writes to it is inhibited.
-STEP	87	O	48mA*	**Step.** This open-drain, high-drive output produces a pulse at a software-programmable rate to move the head during a seek operation.
TC	71	I		**Terminal Count.** This active-high input indicates the end of a DMA transfer. This signal is enabled when the DMA acknowledge pin is active.
-TRK0	97	I		**Track 0.** This active-low input tells the controller that the head is at track zero of the selected disk drive.

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Table 2-1 M5115 Pin Description Table (continued)

Name	Number	Type	Drive Strength*	Description
			Host Bus/ M5115 Configuration	
-RD	15	I		**Read.** When this input is low while the chip is selected, the CPU can read status information or data from the selected register. A buffer may be needed to drive this pin and other external loading depending on specific system implementation. Please see application note.
-WR	14	I		**Write.** When this input is low while the chip is selected, CPU can write control words or data into the selected register. A buffer may be needed to drive this pin and other external loading depending on specific system implementation. Please see application note.
-AEN	12	I		**Address Enable.** When high, this input disables function-selection via A0 ~ A9.
CRB0~4 CRB6~7	41, 43, 44 54, 55, 16, 57	I/O	12mA*	**Configuration Register Bits.** These dual-function pins CRB6~7 act as inputs during reset (if -CRPE = 0) to determine the state of the configuration register bits. The bits of the configuration register is the complement of these inputs. A 10K resistor can be used to pull these pins to the required signal levels. These pins are outputs when the chip is not in reset. These pins have dual functions, as follows: SOUT2/-CRB0, -RTS2/-CRB1, -DTR2/-CRB2, -DTR1/-CRB3, -RTS1/-CRB4, -HCS0/-CRB6, SOUT1/-CRB7.
-CRPE	17	I/O	12 mA*	**Configuration Register Program Enable.** This multifunction pin selects between internal or external default values for the configuration register, and whether the configuration register can be initialized through hardware or software. The chip checks this pin during reset, at that time it acts as an input. If it is low during reset, the configuration register defaults to the complement of the -CPB0~4, 6, 7 pin states. If high, it defaults to 00h. This pin must always have a pull-up or pull-down resistor (10K) attached to pull it to the required signal level. It is driven by the chip when not in reset. Regardless of the initial polarity of this pin, the configuration register can be programmed whenever master reset is inactive.
D0~D7	60~64, 66~68	I/O	21.4mA*	**Data Bus.** This bus contains eight tristate input/ output lines. The bus provides bidirectional communication between the M5115 chip and the CPU. Data, control words, and status information are transferred via the data bus.
R201	83	O		**Game Port Data Read/ PS/2 Bidirection Enable.** This dual-function pin acts as input during reset to determine the state of parallel configuration. If it is high during reset, the parallel defaults to PS/2 software bidirectional parallel port compatible, and if low defaults to PS/2 hardware bidirectional parallel port compatible. The direction depends on the input signal of parallel port pin 38 (-POE). It must have a 10K resistor pull low or up to the required signal level, and acts as output when not in reset cycles. This output pin provides the game port data read enable function in an AT system.

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Table 2-1 M5115 Pin Description Table (continued)

Name	Number	Type	Drive Strength*	Description
			Host Bus/5115 Configuration	
-HOSTIOR	89	O		**-HOSTIOR Buffer Output**. This is the output signal of -IOR.
MR	1	I		**Master Reset.** When high, this input clears all registers, except the parallel port data and status registers (UART receiver buffer, transmitter holding, divisor latch registers). In the flexible disk controller, it resets all disk drive output lines to their disabled state. Reset clears the drive control register, sets the data rate register to 250 kb/s, and sets the main status register to 80. The mode register default values are given in the mode register description. To prevent glitches from activating the reset sequence, attach a CMOS buffer and a 100-pF capacitor to this pin.
OSC1	76	I		**Oscillator.** One side of an external, fundamental 24-MHz crystal is attached here. This pin is tied low if an external clock is used.
OSC2/CLK	75	I/O		**Oscillator/Clock.** One side of an external, fundamental 24-MHz crystal is attached here. If a crystal is not used, a TTL- or CMOS-compatible clock is connected to this pin.
			Power Pins	
VDD	45, 74, 81			**+5 Power.** This is the power supplied to the parallel port, serial ports, FDC digital, FDC analog circuitry, respectively.
VSS	77, 100, 65, 27,			**0V Reference.** This is the reference voltage for the FDC analog, FDC digital, CPU interface, parallel ports, serial port, and disk interface output drive circuitry, respectively.
			UART Control	
-CTS1,	51, 48	I		**Clear to Send.** When low, these inputs indicate to -CTS2 that the modem or data set is ready to exchange data. -CTS is a modem status input whose conditions can be tested by the CPU via reading bit 4 (CTS) of the modem status register (MSR). Bit 4 is the complement of -CTS. Bit 0 (DCTS) of the MSR shows whether -CTS has changed state since the previous reading of the MSR. -CTS has no effect on the transmitter. Whenever the DCTS bit of the MSR changes state, an interrupt is generated if the modem status interrupt is enabled.
-DCD1, -DCD2	52, 47	I		**Data Carrier Detect.** When low, this input indicates that the data carrier has been detected by the modem or data set. The -DCD signal is a modem status input whose condition can be tested by the CPU by reading bit 7 (DCD) of the MSR. Bit 7 is the complement of the DCD signal. Bit 3 (DDCD) of the MSR indicates whether -DCD has changed state since the previous reading of the MSR. Whenever the DCD bit of the MSR changes state, an interrupt is generated if the modem status interrupt is enabled. -DCD has no effect on the receiver.

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Table 2-1 M5115 Pin Description Table (continued)

Name	Number	Type	Drive Strength*	Description
				UART Control
-DSR1, -DSR2	53, 46	I		**Data Set Ready.** When low, this input indicates that the modem or data set is ready to establish communication links with the UART. -DSR signal is a modem status input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MSR. Bit 5 is the complement of -DSR. Bit 1 (DSR) of the MSR shows whether -DSR has changed state since the previous reading of the MSR.
-DTR	54, 44	O	10.7mA*	**Data Terminal Ready.** When low, this output informs the modem or data set that the UART is ready to begin a communications link. -DTR can be set to active-low by programming bit 0 (DTR) of the modem control register (MCR) to a high level. A master reset operation sets this signal to its inactive (high) state.
IRQ3, IRQ4	40, 58	O	10.7mA*	**Interrupt Requests 3 and 4.** These outputs indicate serial port interrupts. The appropriate interrupt goes high whenever it is enabled via the interrupt enable register (IER) and any of the following serial interrupt conditions are active: receiver error flag set, receiver data available, transmitter holding register empty, and modem status set. The interrupt is reset to low upon the appropriate interrupt service, disabling through IER or master reset. IRQ4/ IRQ3 present the interrupt signal if the serial channel is designated COM1/COM2, respectively. Both IRQ3 and IRQ4 can be disabled by resetting OUT 2 low.
RI1, RI2	50, 49	I		**Ring Indicator.** When low, this input indicates that a telephone ringing signal has been received by the modem or data set. -RI is a modem status input whose condition can be tested by the CPU through reading bit 6 (RI) of the MSR. Bit 6 is the complement of -RI. Bit 2 (TERI) of the MSR shows whether -RI has changed state since the previous reading of the MSR. Whenever the RI bit of the MSR changes from a high to a low state, an interrupt is generated if the modem status interrupt is enabled.
BOUT1, BOUT2	57, 41	O	12mA*	**Baud Rate Output.** This multifunction pin gives the associated serial channel baudout signal, after data of 10h has been written to the IIR (interrupt identification register). It also gives the composite serial data output signal for the associated channel after a reset or after 00h is written to IIR.
-RTS1,	55, 43	O	10.7mA*	**Request to Send.** When low, this output indicates to -RTS2, the modem or data set that the UART is ready to exchange data. -RTS can be set to active-low by programming bit 1 (RTS) of the MCR. A master reset operation sets this signal to its inactive (high) state. If -XTSEL is high during reset, loop-mode operation holds this signal in its inactive state. If low, MCR bit 1 controls the associated pin during loop-mode operation.
SIN1, SIN2	56, 42	I		**Serial Input.** This input receives composite serial data from the communications link (peripheral device, modem, or data set).

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Acer Labs: 5F, 156 Min Sheng East Road, Sec. 3, Taipei, Taiwan, ROC Tel: 886-(02) 545-1588 Fax: (02) 719-8691

Table 2-1 M5115 Pin Description Table (continued)

Name	Number	Type	Drive Strength*	Description
			UART Control	
SOUT1, SOUT2	57, 41	O	10.7mA*	**Serial Output.** This output sends composite serial data output to the communications link (peripheral, modem or data set). The SOUT signal is set to the marking (logic 1) state upon a master reset operation.
			Printer Adapter Interface	
-AFD	35	O	16mA*	**Automatic Feed.** When low, this tells the printer to automatically line-feed after each line printed.
BUSY	32	I		**Printer Busy.** This input is set high by the printer when the printer cannot accept another character.
-ERR	28	I		**Error.** This input is set low by the printer when it detects an error.
-INIT	36	O	16mA*	**Initialize.** This active-low output initializes the printer.
PE	30	I		**Paper End.** This input is set high by the printer when it is out of paper.
IRQ7	39	O	16mA*	**Interrupt Request 7.** This output indicates parallel port interrupts. When enabled (control register bit 4 = 1), the appropriate interrupt signal follows the -ACK signal input.
PD0~PD7	26~19	O	16mA*	**Port Data.** These bidirectional pins transfer data to and from the peripheral data bus. These pins have high-current drive capability.
-POE	38	I		**Port Output Enable.** When low, data written to the parallel port data register is output through PD0~PD7. When high, PD0~PD7 are in a high impedance state and act as inputs. This pin is usually tied low for printer operation.
SLCT	29	I		**Select.** This input is set high by the printer when the printer is selected.
-SLIN	37	O	16mA*	**Select Input.** This output selects the printer when the signal is low.
-STB	33	O	6mA*	**Data Strobe.** This output indicates to the peripheral that data at the parallel port is valid.
			IDE Control	
-HSC0, -HSC1	16, 17	O	12 mA*	**Hard Disk Chip Select.** These dual and multifunction outputs provide a fixed disk enable signal when the addresses are present on A0 ~ A9 during a read- or write-access. Using minimal hardware, these signals control and interface between the CPU and a fixed-disk drive that has a controller. -HSC0 is always used for this function after reset, if -XTSEL was high during reset.
-IOCS16	18	I		This AT mode only input signal indicates when 16-bit transfers are to take place. The hard disk interface generates this interface. Logic "0" = 16-bit mode; logic = "1" = 8-bit.

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Table 2-1 M5115 Pin Description Table (continued)

Name	Number	Type	Drive Strength*	Description
				IDE Control
HD7	79	O		**IDE Data Bit 7 in AT Mode.** This is the IDE transfer data at I/O address 1F0H-1F7H (R/W), 3F6 (R/W), 3F7 (W). HD7 connects to IDE data bit 7 when it is the buffer transferring data bit 7 between the IDE and the host during I/O read of 3F7H.
				Game Control
-W201	59	O	12 mA*	This output pin provides the game port data write enable function in AT systems.
-GWR	17	O	12 mA	**Game Write.** This multifunction output provides an active-low signal if I/O address 201h is selected, the write pin is low, and the -XTSEL pin was low during reset. It can be used as a decoded write signal for external logic that implements the game port function in an AT system.
				Miscellaneous
A0 ~ A9	11~2	I		**I/O Address.** Address signals connected to these inputs select the active register during a CPU read or write. See each individual sections (UART, parallel port, FDC, etc.) for details on each register.
CRD1	34	I		This pin acts as input during reset. The logic-level present at this pin, in combination with pin 13 determine the power-on COM port configuration as show below: Power-on hardware configuration of COM port addresses: State of pin 34 during reset / State of pin 13 during reset / UART1 address / UART2 address HI / LO / 3F8 / 2F8 HI / HI / 3F8 / 2E8 LO / LO / 3E8 / 2E8 LO / HI / 2F8 / 3E8
CRD0	13	I		This pin acts as an input pin during hardware reset. The logic-level present at this pin, in combination with pin 34 determines the power-on COM port configuration. See pin 34 description. A 10k resistor can be used to pull this pin to the required signal level.
-XTSEL	18	I		**XT Select.** When this input is low during reset, the chip operates in the XT-compatible mode. When high, it operates in the AT-compatible mode. A pull-down or pull-up resistor must always be attached to this pin.

* *Drive strength specified are for digital outputs at V_{OL1} High. For details, please also refer to DC characteristics in this data sheet.*

Acer Labs: 5F, 156 Min Sheng East Road, Sec. 3, Taipei, Taiwan, ROC Tel: 886-(02) 545-1588 Fax: (02) 719-8691