2.2 Pin Description

Table 2-1 lists the functions of all M5119 pins. A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Table 2-1 M5119 Pin Description Table

Name	Number	Type	Description
HOST Processor Interface			
D0-D7	48-51, 53-56	I/O24	**Data bus**. This connection is used by the host microprocessor to transmit data to and from the M5119. These pins are in a high impedance state when not in the output mode.
IORJ	44	I	**I/O Read**. This active low signal is issued by the host microprocessor to indicate a read operation.
IOWJ	45	I	**I/O Write**. This active low signal is issued by the host microprocessor to indicate a write operation.
AEN	46	I	**Address Enable**. Active high Address Enable indicates DMA operations on the host data bus
A0-A9	28-34, 41-43	I	**I/O Address**. These bits determine the I/O address to be accessed during IORJ and IOWJ cycles.
FDRQ	52	O24	**FDC DMA request**. This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the DACKJ signal going low (or by IORJ going low if DACKJ was already low as in demand mode).
DACKJ	36	I	**DMA acknowledge**. This active low input acknowledging the request for a DMA transfer of data. This input enables the DMA read or write internally.
TC	35	I	**Terminal Count**. This signal indicates to the M5119 that data transfer is complete. TC is only accepted when DACKJ or PDACKJ is low. In AT, TC is active high and in PS/2 mode, TC is active low.
IRQ4 PSPIRQ	38	O24	**Serial Port Interrupt Request**. M5119 (Motherboard application) : This signal is the interrupt from the Primary Serial Port (PSP) or Secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM1 or COM3. The appropriate interrupt from the serial port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. **Primary Serial Port Interrupt**. M5119A (Adapter application) : PSPIRQ is a source of PSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
IRQ3 SSPIRQ	37	O24	**Serial Port Interrupt Request Register**. M5119 (Motherboard application) : IRQ3 is the interrupt from the Primary Serial Port (PSP) or Secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM2 or COM4. The appropriate interrupt from the serial port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. **Secondary Serial Port Interrupt**. M5119A (Adapter application) : SSPIRQ is a source of SSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
FINTR	40	O24	**FDC Interrupt Request**. This interrupt from the Floppy Disk Controller is enabled/disabled via bit 3 of the Digital Output Register (DOR).

Table 2-1 M5119 Pin Description Table (continued)

Name	Number	Type	Description
PINTR	39	O24	**Parallel Port Interrupt Request**. This request from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. If EPP or ECP mode is enabled, this output is pulsed low, then released to allow sharing of interrupts.
RESET	57	IS	**Reset**. This active high signal resets the M5119 and must be valid for 500 ns minimum. In M5119A, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge.
Floppy Disk Interface			
RDATAJ	16	IS	**Read Disk Data.** The active-low, raw data read from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	10	O36	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
WDATAJ	9	O36	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	11	O36	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	7	O36	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
STEPJ	8	O36	**Step.** This active low output produces a pulse at a software-programmable rate to move the head during a seek operation.
DSKCHGJ	17	IS	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
DS0J, DS1J	4, 3	O36	**Drive Select 0, 1**. Active low, output select drives 0-1.
DS2J DS3J PDIR	98	OD36 OD36 O36	**Active low open drain output selects drive 2**. In non-ECP mode : Active low open drain output selects drive 3. This bit is used to indicate the direction of the Parallel port data bus. 0= output/write, 1= input / read. Refer to CR6 bit 2 and bit 3 for further information.
DS3J A10	97	OD36 I	In non-ECP mode, this active-low open drain output selects drive 3. In ECP mode, this pin is the A10 address input.
MTR0J, MTR1J	2, 5	O36	**Motor on 0, 1**. These active-low outputs select motor drives 0-1.
MTR2J PDACKJ	96	OD36 I	**Motor on 2**. This active low open drain output selects motor 2. In ECP mode, MTR2 is the Parallel port DMA acknowledge input.
MTR3J PDRQ	99	OD36 O36	**Motor on 3**. This active low open drain output selects motor 3. In ECP mode, MTR3 is the Parallel Port DMA Request output. This is an active high signal.
DENSEL	1	O36	**Density select**. This signal indicates whether a low (250/300 kbps) or high (500 kbps) data rate has been selected. This is determined by the DENSEL bits in Configuration register 5.
WRTPRTJ	14	IS	**Write Protected**. This active-low Schmitt Trigger input senses from the disk drive that a disk is write-protected. Any write command is ignored.

Table 2-1 M5119 Pin Description Table (continued)

Name	Number	Type	Description
TRK0J	13	IS	**Track 00**. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	12	IS	**Index**. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
DRATE0, DRATE1	19, 18	I/O36	**Data Rate 0, 1**. These two outputs reflect bits 0 and 1 respectively of the Data Rate Register. At power on, these two outputs are in a high impedance state.
Serial Port Interface			
RXD1, RXD2	78, 88	I	**Receive Data**. Receiver serial data input.
TXD1, PCF0	79	O4 I	**Transmit Data**. Transmitter serial data output from Primary Serial Port. **Parallel Port configuration control 0**. M5119A : During reset active, this input signal is read and latched to define the address of the Parallel port.
RTS1J PCF1	81	O4 I	**Request to send**. Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. **Parallel port configuration control 1**. M5119A : During reset active, this input is read and latched to define the address of the Parallel port.
RTS2J S2CF0	91	O4 I	**Request to send**. This active low output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. **Secondary serial port configuration control 0**. M5119A : During reset active, this input is read and latched to define the address of the Secondary serial port.
DTR1J IDECF	83	O4 I	**Data Terminal Ready**. This is an active low output for primary serial port. Handshake output signal signifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation. **IDE Configuration control**. M5119A : When active, this input is read and latched to enable/disable the IDE
DTR2J S2CF1	93	O4 I	**Data Terminal Ready**. This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation. **Secondary serial port configuration control 1**. M5119A : When active, this input is read and latched to define the address of the Secondary Serial port.
TXD2 FDCCF	89	O4 I	**Transmitter Serial Data output from Secondary Serial Port**. **Floppy Disk Configuration**. M5119A : This input is read and latched during Reset to enable/disable the Floppy Disk Controller.

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Table 2-1 M5119 Pin Description Table (continued)

Name	Number	Type	Description
CTS1J CTS2J	82, 92	I	**Clear to Send**. This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 Modem status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	80, 90	I	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	85, 87	I	**Data Carrier Detect**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state changes from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. **Note** : bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	84, 86	I	**Ring Indicator**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note: bit 6 of MSR is the complement of RIJ.
DRV2 ADRxJ PINTR2 ECPEN	94	I O24 O24 I	**Drive 2**. In PS/2 mode, this input indicates whether a second drive is connected; this signal should be low if a second drive is connected. This status is reflected in a read of Status Register A. (Only available in M5119. This pin must not be driven in the M5119A) **Optional I/O port address decode output**. Defaults to tri-state after power-up. This pin has 30 µA internal pull-up. This interrupt from the parallel port enabled/disabled via bit 4 of the Parallel Port Control Register. Refer to Configuration Registers CRC for more information. **Enhanced parallel port mode select**. M5119A : Read and latched during reset active.
SLCTINJ	73	O20	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
INITJ	74	O20	**Initiate Output**. This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
AUTOFDJ	76	O20	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.

Table 2-1 M5119 Pin Description Table (continued)

Name	Number	Type	Description
STROBEJ	77	O20	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	61	I	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	62	I	**Acknowledge**. This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	60	I	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	59	I	**Printer Selected Status**. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	75	I	**Error**. This active low signal indicates an error condition at the printer.
PD0-PD7	71-68, 66-63	I/O20	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
IOCHRDY	100	OD24	**IOCHRDY**. In EPP mode, this pin is pulled low to extend the read/write command.
IDE			
IDEENLOJ SICF1	23	O24 I	**IDE Low Byte enable**. This active low signal is used in AT mode. During AT mode, this pin is active when the IDE is enabled and the I/O address is accessing 1F0H~1F7H and 3F6H~3F7H in primary address mode or 170H-177H and 376H, 377H in secondary address mode. **Primary Serial Configuration 1**. M5119A : Read and latched during reset active to select the address of the Primary Serial Port.
IDEENHIJ SICF0	24	O24	**IDE High Byte Enable**. This active low signal is effective in AT mode, and when IO16CSB is also active. The I/O addresses for which this pin reacts are 1F0h-1F7h in primary address mode or 170h-177h in secondary address mode. **Primary Serial Configuration 0**. M5119A : Read and latched during reset active to define the address of the Primary Serial Port.
HDCS0J IDEACF	25	O16	**Hard Disk Chip Select**. This signal corresponds to addresses 1F0H-1F7H in primary address mode or 170H-177H in secondary address mode in the AT mode. **IDE address control**. M5119A : Read and latched during reset active.
HDCS1J FACF	26	O16	**Hard Disk Chip Select**. This active low signal corresponds to 3F6h, 3F7h for primary address mode or 376h, 377h for secondary address mode in the AT mode. **Floppy Disk Address Control**. M5119A : This signal is read and latched during reset active.
IOCS16J	27	I	**I/O 16-bit Indicator**. This active low signal indicates 16-bit transfers are to take place. This signal is generated by the harddisk interface. 8 bit mode indicates this signal is high.
IDED7	22	I/O24	**IDE data bit 7 in AT mode**. IDED7 transfers data at I/O addresses 1F0h-1F7h(R/W), 3F6(R/W), 3F7(W). IDED7 should be connected to IDE data bit 7. The M5119 acts as a buffer transferring data bit 7 between the IDE

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Table 2-1 M5119 Pin Description Table (continued)

Name	Number	Type	Description
Miscellaneous			
PWRGD	58	I	**Power Good**. M5119 : This input signal indicates that the power is valid. For device operation, PWRGD must be active.
GAMECSJ		O4	**Game port chip select**. M5119A : This active low output will be active when the I/O address is 201h.
PADCF			**Parallel port mode control**. M5119A : This active high signal is read and latched during reset active.
X1/CLK1	20	ICLK	**Clock 1**. This external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
X2/CLK2	21	OCLK	**Clock 2**. This is a 24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
Vcc	15, 72		**Power**. +5 Volt supply pin.
Vss	6, 47, 67, 95		**Ground pins**.

Type Descriptions :

I	Input TTL compatible
IS	Input with Schmitt Trigger
I/O20	Input/Output with 20 mA sink @ 0.4 V, source 8 mA @ 2.4 V
I/O24	Input/Output with 24 mA sink @ 0.4 V, source 8 mA @ 2.4 V
I/O36	Input/Output with 36 mA sink @ 0.4 V, source 8 mA @ 2.4 V
ICLK	CLK input at 24 MHz
OCLK	CLK output at 24 MHz
O4	Output with 4 mA sink @ 0.4 V, source 4 mA @ 2.4 V
O16	Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V
O20	Output with 20mA sink @ 0.4 V, source 8 mA @ 2.4 V
O24	Output with 24mA sink @ 0.4 V; source 12 mA @ 2.4 V.
O36	Output with 36 mA sink @ 0.4 V; source 8 mA @ 2.4 V.
OD24	Open drain outputs, sinks 24 mA @ 0.4 V
OD36	Open drain outputs, sinks 36 mA @ 0.4 V.