Section 2 : Pin Description

2.1 Pinout Diagram

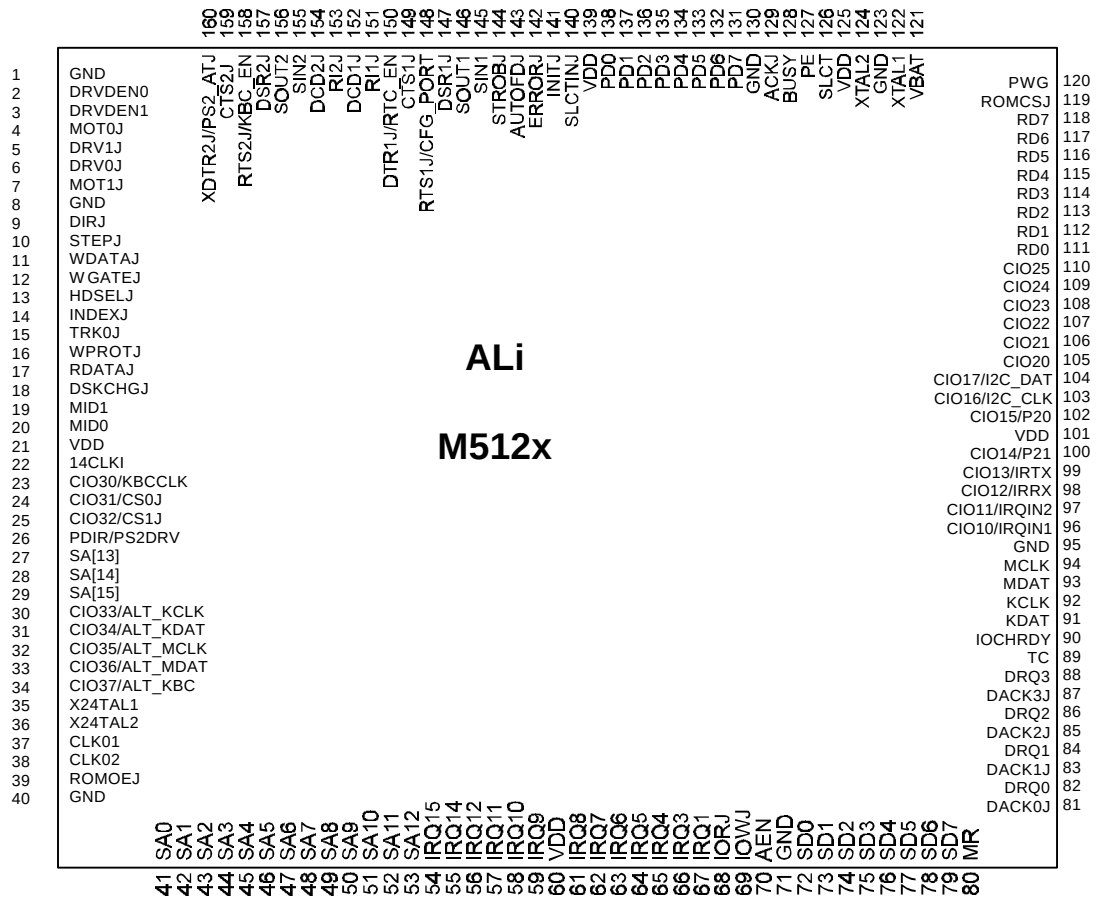

Figure 2-1. M512x Pin Diagram

2.2 Pin Description

Table 2-1 lists the functions of all M512x pins. A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Table 2-1 M512x Pin Description Table

Name	Number	Type	Description
HOST Processor Interface			
SD0-SD7	70-72	I/O24	**Data bus**. This connection is used by the host microprocessor to transmit data to and from the M512x. These pins are in high impedance state when not in the output mode.
IORJ	68	I	**I/O Read**. This active low signal is issued by the host microprocessor to indicate a read operation.
IOWJ	69	I	**I/O Write**. This active low signal is issued by the host microprocessor to indicate a write operation.
AEN	70	I	**Address Enable**. This active high signal indicates DMA operations on the host data bus.
SA0-SA15	41-53, 27-29	I	**I/O Address**. These bits determine the I/O address to be accessed during IORJ and IOWJ cycles.
DACK0J-DACK3J	81,83,85,87	I	**DMA Acknowledge.** An active low input signal acknowledging the request for a DMA data transfer. This input enables the DMA read or write internally.
DRQ0-DRQ3	82,84,86,88	O24	**DMA request**. This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the DACKJ signal going low (or by IORJ going low if DACKJ was already low as in demand mode).
TC	89	I	**Terminal Count**. This signal indicates to the M512x that data transfer is complete. TC is only accepted when DACKJ is low. In AT mode, TC is active high and in PS/2 mode, TC is active low.
IRQ1, IRQ3-12, IRQ14-15	67,66,65,64, 63,62,61,59, 58,57,56,55, 54	O24	**Interrupt Requests**.
MR	80	IS	**Reset**. This active high signal resets the M512x and must be valid for 500 ns minimum. In M512x, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge.
Floppy Disk Interface			
RDATAJ	17	IS	**Read Disk Data.** The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	12	O36	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
WDATAJ	11	O36	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	13	O36	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	9	O36	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.
STEPJ	10	O36	**Step.** This active low output produces a pulse at a software-programmable rate to move the head during a seek operation.
DSKCHGJ	18	IS	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Floppy Disk Interface			
DRV0J, DRV1J	6, 5	O36	**Drive Select 0, 1**. Active low, output select drives 0-1.
PDIR PS2DRV	26	O4 I	This bit is used to indicate the direction of the Parallel port data bus. 0= output/write, 1= input / read. **Drive 2**. In PS/2 mode, this input indicates whether a second drive is connected; this signal should be low if a second drive is connected. This status is reflected in a read of Status Register A.
MID0-1	20,19	IS	**Media ID inputs.** In floppy enhanced mode, these inputs are the media ID inputs.
MOT0J, MOT1J	4, 7	O36	**Motor on 0, 1**. These active-low outputs select motor drives 0-1.
WPROTJ	16	IS	**Write Protected**. This active-low Schmitt Trigger input senses from the disk drive that a disk is write-protected. Any write command is ignored.
TRK0J	15	IS	**Track 00**. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	14	IS	**Index**. This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
DRVDEN 0-1	2-3	O36	**Data Rate 0-1**. This output reflects bits 0-1 of the Data Rate Register.
Serial Port Interface			
SIN1, SIN2	145,155	I	**Receive Data**. Receiver serial data input.
SOUT1, SOUT2	146,156	O4	**Transmit Data**. Transmitter serial data output from Serial Port.
RTS1J CFGPORT	148	O4 I	**Request to send**. Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. **Configuration port select**. During reset active, this input is read and latched to define the configuration register's base address.
RTS2J KBC_EN	158	O4 I	**Request to send**. This active low output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation. **KBC enable control**. During reset active, this input is read and latched to enable KBC after reset. The enable could be overwritten by configuration register.
DTR1J RTC_EN	150	O4 I	**Data Terminal Ready**. This is an active low output for primary serial port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation. **RTC enable control**. During reset active, this input is read and latched to enable RTC after reset. The enable could be overwritten by configuration register.

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Serial Port Interface			
DTR2J	160	O4	**Data Terminal Ready**. This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation.
PS2_ATJ		I	**KBC PS2 mode or AT mode select** When active, this input is read and latched to define the KBC PS-2 or AT mode.
CTS1J CTS2J	149, 159	I	**Clear to Send**. This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	147, 157	I	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	152, 154	I	**Data Carrier Detect** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state changes from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. Note : bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	151, 153	I	**Ring Indicator**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note : bit 6 of MSR is the complement of RIJ.

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Printer Port Interface			
AUTOFDJ	143	O20	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
INITJ	141	O20	**Initiate Output**. This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
SLCTINJ	140	O20	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
STROBEJ	144	O20	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	128	IS	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	129	IS	**Acknowledge**. This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	127	IS	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	126	IS	**Printer Selected Status**. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	142	O20	**Error**. This active low signal indicates an error condition at the printer.
PD0-PD7	138-131	I/O20	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
IOCHRDY	90	OD24	**IOCHRDY**. In EPP mode, this pin is pulled low to extend the read/write command.
Real-Time Clock			
XTAL1	122	ICLK	**32Khz Crystal Input**
XTAL2	124	OCLK	**32Khz Crystal Output**
VBAT	121	P	**Battery Voltage.**
PWG	120	IS	**Power Good Input.**
Keyboard Controller			
KDAT	91	I/O24	**Keyboard Data.**
KCLK	92	I/O24	**Keyboard Clock.**
MDAT	93	I/O24	**Mouse Data.**
MCLK	94	I/O24	**Mouse Clock.**

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
BIOS Buffer			
ROMOEJ	39	IS	**ROM Output Enable.**
ROMCSJ	119	IS	**ROM Chip Select.**
RD0-7	111-118	I/O4	**ROM Bus.**
Common I/O			
CIO10-11	96-97	I/O4 I	**Common I/O.** **IRQ In.**
CIO12	98	I/O4 I	**Common I/O.** **IRRX.**
CIO13	99	I/O8 O	**Common I/O.** **IRTX.**
CIO14	100	I/O4 O	**Common I/O.** **KBC P21 function.**
CIO15	102	I/O4 O	**Common I/O.** **KBC P20 function.**
CIO16	103	I/O4 O	**Common I/O.** **I^2C_CLK.**
CIO17	104	I/O4 I/O4	**Common I/O.** **I^2C_DAT.**
CIO20-24	105-109	I/O4	**Common I/O.**
CIO25	110	I/O4 I	**Common I/O.** **KEYLOCKJ.**
CIO30	23	I/O4 I	**Common I/O.** **KBC_CLK.**
CIO31	24	I/O8 O	**Common I/O.** **General Chip Select decoder CS0J.**
CIO32	25	I/O8 O	**Common I/O.** **General Chip Select decoder CS1J.**
CIO33	30	I/O16 O	**Common I/O.** **Alternative Keyboard Clock.**
CIO34	31	I/O16 O	**Common I/O.** **Alternative Keyboard Data.**
CIO35	32	I/O16 O	**Common I/O.** **Alternative Mouse Clock.**
CIO36	33	I/O16 O	**Common I/O.** **Alternative Mouse Data.**
CIO37	34	I/O4 I	**Common I/O.** **Alternative KBC select.**

Table 2-1 M512x Pin Description Table (continued)

Name	Number	Type	Description
Miscellaneous			
X24TAL1	35	ICLK	**Clock 1**. This external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
X24TAL2	36	OCLK	**Clock 2**. This is a 24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
X14CLKI	22	I	**Clock 14 In**. This is a 14.318 MHz clock source in.
XCLKO1	37	O	**Clock 14 out**. This is a 14.318 MHz clock out.
XCLKO2	38	O	**Clock 14 out**. This is the second 14.318 MHz clock out.
Power Pins			
Vcc	21,60,101, 139	P	**Power**. +5 Volt supply pin.
Vss	1,8,40,71,95, 130,139	P	**Ground pins**.

Type Description :

I	Input TTL compatible.
IS	Input with Schmitt Trigger.
I/O16	Input/Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
I/O20	Input/Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V.
I/O24	Input/Output with 24 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
ICLK	CLK input.
OCLK	CLK output.
O4	Output with 4 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
O8	Output with 8 mA sink @ 0.4 V, source 4 mA @ 2.4 V.
O16	Output with 16 mA sink @ 0.4 V, source 8 mA @ 2.4 V.
O20	Output with 16 mA sink @ 0.4 V, source 16 mA @ 2.4 V.
O24	Output with 24 mA sink @ 0.4 V; source 12 mA @ 2.4 V.
O36	Output with 36 mA sink @ 0.4 V; source 4 mA @ 2.4 V.
OD24	Open drain outputs, sinks 24 mA @ 0.4 V.