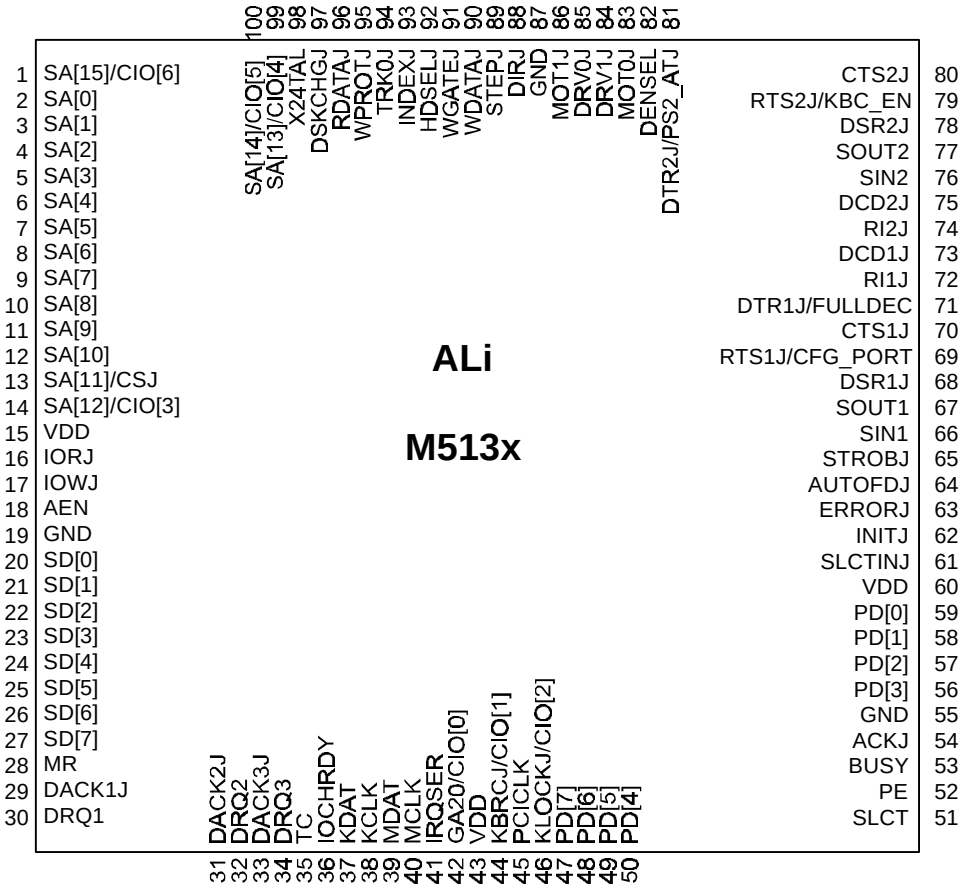
Section 2 : Pin Description

2.1 Pinout Diagram



2.2 Pin Description

Table 2-1 lists the functions of all M513X pins. A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Table 2-1 M513X Pin Description Table

Name	Number	Type	Description
HOST Processor Interface :			
SD0-SD7	20-27	I/O16	**Data bus**. This connection is used by the host microprocessor to transmit data to and from the M513X. These pins are in high impedance state when not in the output mode.
IORJ	16	IS	**I/O Read**. This active low signal is issued by the host microprocessor to indicate a read operation.
IOWJ	17	IS	**I/O Write**. This active low signal is issued by the host microprocessor to indicate a write operation.
AEN	18	IS	**Address Enable**. This active high signal indicates DMA operations on the host data bus.
SA0-SA10	2-12	IS	**I/O Address**. These bits determine the I/O address to be accessed during IORJ and IOWJ cycles.
SA[11]/CSJ	13	IS	**Chip Select.** This is the chip select signal to qualify SA[11-15] if the full decoder function is not selected. If the full decoder function is selected, this pin should be connected to SA[11].
DACK1J-DACK3J	29,31,33	IS	**DMA Acknowledge.** An active low input signal acknowledging the request for a DMA data transfer. This input enables the DMA read or write internally.
DRQ1-DRQ3	30,32,34	O16	**DMA request**. This active high output is the DMA request for byte transfers of data to the host. This signal is cleared on the last byte of the data transfer by the DACKJ signal going low (or by IORJ going low if DACKJ was already low as in demand mode).
TC	35	IS	**Terminal Count**. This signal indicates to the M513X that data transfer is complete. TC is only accepted when DACKJ is low. In AT mode, TC is active high and in PS/2 mode, TC is active low.
IRQSER	41	I/O16	**Serial Interrupt Requests**. Serial interrupt encoder signal.
PCICLK	45	I	**PCI Clock Input.** This signal typically is a 33 Mhz signal used to synchronize the serial interrupt signal between the host and devices.
MR	28	IS	**Reset**. This active high signal resets the M513X and must be valid for 500 ns minimum. In M513X, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge.
IOCHRDY	36	OD16	**IOCHRDY**. In EPP mode, this pin is pulled low to extend the read/write command.
Floppy Disk Interface			
RDATAJ	96	IS	**Read Disk Data.** The active-low, raw data read signal from the disk is connected here. Each falling edge represents a flux transition of the encoded data.
WGATEJ	91	O36	**Write Gate**. This active-low, high-drive output enables the write circuitry of the selected disk drive. This signal prevents glitches during power-up and power-down. This prevents writing to the disk when power is cycled.
WDATAJ	90	O36	**Write Data**. This active low output is a write- precompensated serial data to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
HDSELJ	92	O36	**Head Select**. This active low output determines which disk drive head is active. Low = Head 0, high (open) = Head 1.
DIRJ	88	O36	**Direction.** This active low output determines the direction of the head movement (low = step-in, high = step-out). During the write or read modes, this output is high.

Table 2-1 M513X Pin Description Table (continued)

Name	Number	Type	Description
Floppy Disk Interface			
STEPJ	89	O36	**Step.** This active low output signal produces a pulse at a software-programmable rate to move the head during a seek operation.
DSKCHGJ	97	IS	**Disk Change.** This disk interface input indicates when the disk drive door has been opened. This active-low signal is read from bit D7 of address xx7h.
DRV0J, DRV1J	85,84	O36	**Drive Select 0, 1**. Active low, output select drives 0-1.
MOT0J, MOT1J	83,86	O36	**Motor on 0, 1**. These active-low outputs select motor drives 0-1.
WPROTJ	95	IS	**Write Protected**. This active-low Schmitt Trigger input signal senses from the disk drive that a disk is write-protected. Any write command is ignored.
TRK0J	94	IS	**Track 00**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the outermost track.
INDEXJ	93	IS	**Index**. This active low Schmitt Trigger input signal senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
DENSEL	82	O36	**Density Select**. Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.
Serial Port Interface			
SIN1, SIN2	66,76	IS	**Receive Data**. Receiver serial data input signal.
SOUT1, SOUT2	67,77	O4	**Transmit Data**. Transmitter serial data output from Serial Port.
RTS1J	69	O4	**Request to send**. Active low Request to send output for Primary Serial port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
CFGPORT		I	**Configuration port select**. During reset active, this input is read and latched to define the configuration register's base address. This pin has a 20K(default) internal pull-up resistor.
RTS2J	79	O4	**Request to send**. This active low output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will clear the RTSJ signal to inactive mode (high). Forced inactive during loop mode operation.
KBC_EN		I	**KBC enable control**. During reset active, this input is read and latched to enable KBC after reset. The enable could be overwritten by configuration register. This pin has a 20K(default) internal pull-up resistor.
DTR1J	71	O4	**Data Terminal Ready**. This is an active low output for primary serial port. Handshake output signal signifies to modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive during loop mode operation.
FULLDEC		I	**Full decoder enable**. During reset active, this input is read and latched to determine whether a fully decoder (SA15-SA11) is supported. This pin has a 20K(default) internal pull-up resistor.

Table 2-1 M513X Pin Description Table (continued)

Name	Number	Type	Description
Serial Port Interface			
DTR2J	81	O4	**Data Terminal Ready**. This active low output is for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will clear the DTRJ signal to inactive mode (high). Forced inactive during loop mode operation.
PS2_ATJ		I	**KBC PS2 mode or AT mode select** When active, this input is read and latched to define the KBC PS-2 or AT mode. This pin has a 20K(default) internal pull-up resistor.
CTS1J CTS2J	70,80	IS	**Clear to Send**. This active low input for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of CTSJ signal by reading bit 4 of Modem Status Register (MSR). A CTSJ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when CTSJ changes state. The CTSJ signal has no effect on the transmitter. Note : Bit 4 of MSR is the complement of CTSJ.
DSR1J DSR2J	68,78	IS	**Data Set Ready.** This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of DSRJ signal by reading bit5 of Modem Status Register (MSR). A DSRJ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DSRJ changes state. Note: Bit 5 of MSR is the complement of DSRJ.
DCD1J, DCD2J	73,75	IS	**Data Carrier Detect**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of DCDJ signal by reading bit 7 of Modem Status Register (MSR). A DCDJ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when DCDJ changes state. Note : bit 7 of MSR is the complement of DCDJ.
RI1J, RI2J	72,74	IS	**Ring Indicator**. This active low input is for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of RIJ signal by reading bit 6 of Modem Status Register (MSR). An RIJ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when RIJ changes state. Note : bit 6 of MSR is the complement of RIJ.

Table 2-1 M513X Pin Description Table (continued)

Name	Number	Type	Description
Printer Port Interface			
AUTOFDJ	64	O20	**Autofeed Output**. This active low output causes the printer to automatically feed one line after each line is printed. This signal is the complement of bit 1 of the Printer Control Register.
INITJ	62	O20	**Initiate Output**. This active low signal is bit 2 of the printer control register. This is used to initiate the printer when low.
SLCTINJ	61	O20	**Printer select input**. This active low signal selects the printer. This is the complement of bit 3 of the Printer Control Register.
STROBJ	65	O20	**Strobe Output**. This active low pulse is used to strobe the printer data into the printer. This output signal is the complement of bit 0 of the Printer Control Register.
BUSY	53	IS	**Busy**. This signal indicates the status of the printer. A high indicates the printer is busy and not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.
ACKJ	54	IS	**Acknowledge**. This active low output from the printer indicates it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the ACKJ input.
PE	52	IS	**Paper End**. This signal indicates that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
SLCT	51	IS	**Printer Selected Status**. This active high output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
ERRORJ	63	O20	**Error**. This active low signal indicates an error condition at the printer.
PD0-PD7	59-56,50-47	I/O20	**Port Data**. This bi-directional parallel data bus is used to transfer information between CPU and peripherals.
Keyboard Controller			
KDAT	37	I/O24	**Keyboard Data.**
KCLK	38	I/O24	**Keyboard Clock.**
MDAT	39	I/O24	**Mouse Data.**
MCLK	40	I/O24	**Mouse Clock.**
Common I/O			
CIO0	42	I/O4 O4	**Common I/O.** **KBC P21 (GATE A20) function.**
CIO1	44	I/O4 O4	**Common I/O.** **KBC P20 (KBC_RST) function.**
CIO2	46	I/O4 IS	**Common I/O.** **KBC P17 (KEYLOCKJ) function.**
CIO3	14	I/O4 IS	**Common I/O.** **SA[12]/PS2DRV/IRQIN**
CIO4	99	I/O4 IS O	**Common I/O.** **SA[13]** **PDIR/DRVDEN1**
CIO5	100	I/O4 IS	**Common I/O.** **SA[14]/IRRX2/MEDIA_ID0**
CIO6	1	I/O4 IS O4	**Common I/O.** **SA[15]/MEDIA_ID1** **IRTX2**
Miscellaneous			
X24TAL	98	I	**Clock 1**. This external connection for a 24 MHz CMOS compatible oscillator.
VDD	15,43,60	P	**Power**. +5 Volt supply pin.
GND	19,55,87	P	**Ground pins**.